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Performance Investigation of Dual-Halo Dual-Dielectric Triple Material Surrounding Gate MOSFET with High-κ dielectrics for Low Power Applications

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Abstract—**The rapidly growth in semiconductor industry puts huge demand of scalable devices with low standby power for future VLSI chips. The further mitigation in device dimension becomes a challenging task due to the existence of unavoidable short channel effects. The introduction of gate stack and channel engineering in MOSFET devices open a new window for future generation devices. This paper presents gate stack structure with low-κ dielectric material as silicon oxide and replacement of various high-κ dielectric materials to analyze the device performance. The unification of new oxide material in the device enhances the immunity against SCEs and improves the gate leakage current. Dual-Halo Dual-Dielectric Triple Material Surrounding Gate (DH-DD-TM-SG) MOSFET has shown better performance with high dielectric constant materials. The device exhibits more value of transconductance with high-κ dielectrics.**

Index Terms—**Channel engineering, gate stack engineering, high-κ materials, short channel effects, MOSFETs**

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I. INTRODUCTION

The mobile communication and telecom sectors are the fastest growing fields. The customer demands high speed, small size, and low power consumption devices. But conventional MOSFET has reached its scaling limit due to existence of various short channel effects (SCEs) [1]. A new method must be found out to satisfy the high demands in the electronics world. Finally, a viable solution has emerged, with gate stack and channel engineering in the DH-DD-TM-SG MOSFET. This development in MOSFET has become the most suitable choice for the next generation devices. But, carry new challenges and opportunities for manufacturing and design. Gate stack structure is scrutinized with high dielectric materials to diminish leakage current [2, 3]. The Hafnium oxide is proposed as an alternate choice for gate oxide owing to its better thermal stability. Gate stack have equivalent oxide thickness (EOT) of 1.78 nm with insignificant leakage through gate oxide [4]. Researchers have advised numerous high-κ dielectric materials for gate oxide which consists of hafnium-based oxide and aluminum-based oxides [5]. The basic properties of good dielectrics are insulation and formation of capacitance. The band offset value should be more than 1ev to reduce the carrier injections in the bands. Good Thermal stability and high re-crystallization temperature should also possess by the oxide materials [6-8]. The density of interface trap charges diminishes with a narrow interfacial oxide layer in gate stack. The field inside the channel boosts up and significant reduction in leakage current is observed in

gate stack [9]. Depending upon all these requirements, five dielectric materials are considered for the present investigation. In the literature, the suitable range of band gap is reported as 5.16 to 7.8 eV [10, 11]. The properties of various high-κ dielectric materials are reported by Nirmal et al. [12]. The band gap of silicon oxide is very high and for titanium oxide is very low in contrast to requirements. So, hafnium oxide is suitable material for gate stack structure along with silicon oxide. It shows higher degree of potential at higher temperature condition for MOSFET.

The manufacturing viability of proposed device using different approaches is available in literature. The triple metal has been fabricated by utilizing Molybdenum (Mo) acting as gate material as its work function can be change by varying N_2 implant. Cylindrical gate stack source and drain is formed by using deep trench etching. Dual dielectric is formed by deposition of oxide layers. Similar types of devices were fabricated in the literature. However, fabrication of proposed structure has not yet done [13-16].

DH-DD-TM-SG MOSFET has been promising device for mixed signal applications due to cutback in SCEs and leakage current. Distinct high dielectric constant materials are utilized in the device and comparison has been carried out among their performances. Short channel behavior of proposed device has been investigated and proposed device reveals outperform performance. Atlas device simulator is used for the simulation. The proposed device is designed and simulated to find out various short channel performance metrics. The effect of high-κ dielectric is examined by substituting the oxide in the gate stack. The hafnium oxide shows an excellent performance with amended transconductance and drain current.

II. Analytical Model

Fig. 1(a) and (b) depicts the exploded diagram of DH-DD-TM-SG MOSFET and simulated structure in device simulator. Channel engineering is incorporated at gate electrode using three different gate materials with changed work function of metals. The work function of metals are ϕ_{M1} = 4.8 eV (Au), ϕ_{M2} = 4.6 eV (Mo) and ϕ_{M3} = 4.4 eV (Ti) respectively. It improves the carrier transportation efficiency and current. If order of metal work functions is changed then impact ionization occurs and device performance degrades [17, 18].

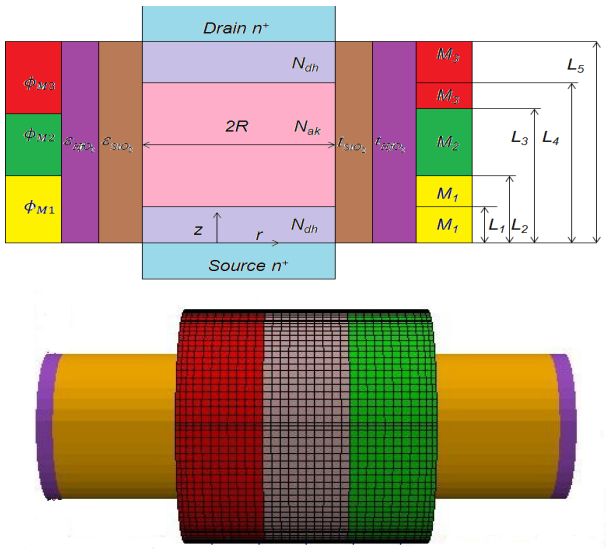

Fig. 1. (a) Cross sectional view of proposed device, (b) Simulated structure of the proposed device.

Gate stack consist of two dielectrics which improves the sub-threshold behavior of the device. The symmetric dual halo doping is integrated into the structure which reduces the SCEs.

(1) Surface Potential

The electrostatic potential formed by surface confined charges is known as the surface potential. The Poisson's equation is used to determine the potential in the channel. It is given as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\left[\phi_p(r,z)\right]}{\partial r}\right)+\frac{\partial^2\left[\phi_p(r,z)\right]}{\partial z^2}=\frac{qN_{ap}}{\varepsilon_{Si}}$$
$$(L_{p-1}\le z\le L_p) \qquad (1)$$

where p=1, 2, 3, 4, 5

The parabolic approximation is used to calculate the potential distribution and is given by [19].

$$\phi(r,z)=\chi_0(z)+\chi_1(z)\mathrm{r}+\chi_2(z)\mathrm{r}^2 \qquad (2)$$

where the value of constant $\chi_0(z)$, $\chi_1(z)$ and $\chi_2(z)$ can be achieved by using boundary conditions given by [9]. Potential is given as

$$\frac{d^2\phi_{sp}(z)}{dz^2}-\phi_{sp}(z)\left(\frac{2C_{oxdh}}{\varepsilon_{Si}R}\right)+(\mathrm{VGS}-V_{fbp})\left(\frac{2C_{oxdh}}{\varepsilon_{Si}R}\right)=\frac{qN_{ap}}{\varepsilon_{Si}} \tag{3}$$

C_{oxdh} is the gate oxide capacitance.

$$C_{oxdh}=\frac{\varepsilon_{SiO_2}}{R\ln\left[1+\frac{t_{oxdh}}{R}\right]} \tag{4}$$

where t_{oxdh} is the gate oxide thickness [20].

$$t_{oxdh}=t_{SiO_2}+\frac{\varepsilon_{SiO_2}}{\varepsilon_{High-\kappa}}t_{High-\kappa} \tag{5}$$

Value of $\varepsilon_{High-\kappa}$ is changes according to dielectric materials. The Eq. (3) Can be written as:

$$\frac{d^2\phi_{sp}(z)}{dz^2}-\theta^2\phi_{sp}(z)=\chi_p \tag{6}$$

The solution of Eq. (6) is given as

$$\phi_{sp}(z)=\alpha_p e^{(\theta z)}+\beta_p e^{(-\theta z)}-\frac{\chi_p}{\theta^2} \tag{7}$$

where $\theta^2=\frac{2C_{oxdh}}{\varepsilon_{Si}R}$

$$\chi_p=\frac{qN_{ap}}{\varepsilon_{Si}}-\theta^2(\mathrm{VGS}-\mathrm{v}_{fbp})$$

where α_p & β_p are arbitrary constants, continuity equations for the potential (ϕ) and field (E) are used to find out value of constants [9].

(2) Electric Field

The electric field is extracted by differentiating potential w.r.t. z.

$$E_{\mathrm{p}(z)}=-\frac{d\phi_{sp}(z)}{dz}=\theta(\beta_p e^{(-\theta z)}-\alpha_p e^{(\theta z)}) \tag{8}$$

(3) Threshold Voltage

The device turns ON voltage is threshold voltage which is twice the Fermi potential and equal to the minimum surface potential.

$$\phi_{\min sp}=2\phi_f \tag{9}$$

$$2\sqrt{\alpha_1\beta_1}-\frac{\chi_1}{\theta^2}=2\frac{KT}{q}\ln\left(\frac{N_{ap}}{n_i}\right)\Bigg|_{VGS=v_{th}} \tag{10}$$

At the location of ϕ_{minsp}, the sub-threshold leakage current starts in the device. So, it is very useful for modeling of the threshold voltage.

Table 1. summarizes the device parameters used for simulation

Parameters	DH-DD-TM-SG
S/D Doping ($/m^3$)	$1x10^{26}$
Channel Doping ($/m^3$)	$1x10^{23}$
Halo Doping ($/m^3$)	$1x10^{24}$
T_{ox} (nm)	1.78
T_{Si} (nm)	10
Channel Length (nm)	30
Permittivity of SiO_2	3.9
Permittivity of Al_2O_3	8
Permittivity of $LaAlO_3$	15
Permittivity of HfO_2	21
Permittivity of TiO_2	40
VGS	0.2 V
VDS	0.1 V

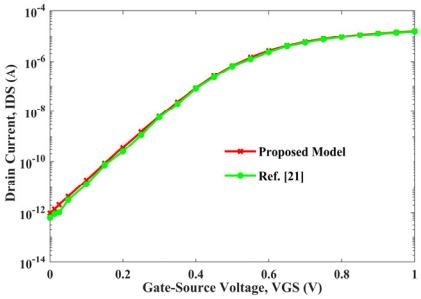

Fig. 2. Calibration of proposed device results with experimental results.

III. RESULTS & DISCUSSION

The device parameters used during simulation are listed in Table 1.

The simulated data of proposed model is calibrated with the simulated work [21] which validates the models used for the device simulation. Fig. 2 depicts that simulated results are well matched with the experimental results.

1. Surface Potential

The present analysis is carried out for surface potential ϕ_{sp} . The different metal work function produces step potential profile which minimizes the SCEs and screening of a channel province under high metal work function from the variation in the drain potential. The lower metal gate work function near to drain side absorbs the extra drain bias variation which mitigates the DIBL [22, 23]. The difference in work function among the interfaces of metals creates the step up in the potential profile. Fig. 3 shows that triple material structure has two step function profile which is a clear indication of a reduction in SCEs. These gradual steps function profile at the interface screens the higher metal gate M_1 work function region from the fluctuation of drain potential. Enhanced *VDS* is discarded across the lower metal gate M_3 work function region. It is noticed that the minimum surface potential ϕ_{sp} happens for DH-DD-TM-SG MOSFET in the halo region. In this novel device, there are additional steps at the drain and source sides. Normally, there are two step function profiles in TM-SG but for dual halo, it is realized that the surface potential of DH-DD-TM-SG exhibits four step function profiles. So, this extra step profile further helps in scale down the short channel influence and improving the current driving capability. The analytical results are well in agreement with simulated results validating the model [24]. Fig. 3 highlights the potential of proposed device with different values of κ. The step rise in potential is observed in halo doped region of 1.05 V as compared to the rest of the portion which shows potential of 0.78 V which is due to sudden change in doping. The value of surface potential is more for Al_2O_3 as compared to other dielectrics due to its lower physical thickness. TCAD Silvaco is used for extracting the simulation data and MATLAB is used for plotting and solving mathematical equations [25].

2. Electric Field

Fig. 4 reveals the field of DH-DD-TM-SG MOSFET with various dielectric constants. It is also observed from the figure that the increase in κ values enhances the field in the channel. The extra peak of field is detected at the interfaces of metals. These peaks decrease the field at drain terminal which causes diminution in DIBL and hot carrier effects. These are the prime SCEs in MOSFET which reduces its performance at lower dimension.

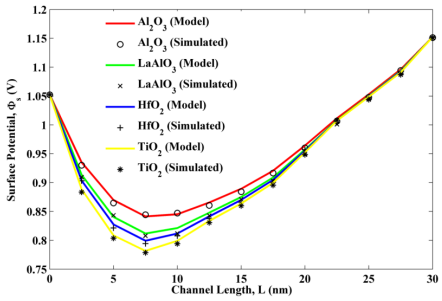

Fig. 3. Potential of proposed device with various dielectric materials.

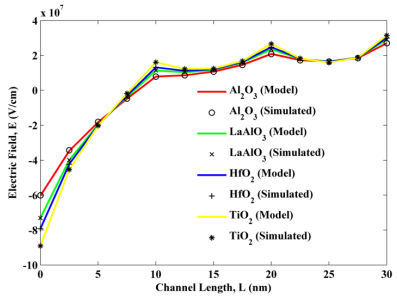

Fig. 4. Field of proposed device with various dielectric materials.

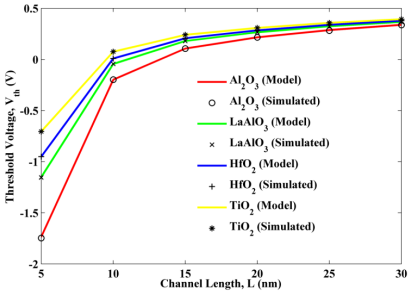

Fig. 5. Threshold voltage of proposed device with various dielectric materials.

3. Threshold Voltage

Fig. 5 shows the threshold voltage of DH-DD-TM-SG MOSFET. It is also observed from the figure that the increase in κ values enhances the threshold voltage. Lower value of threshold voltage of a device increases the leakage current and higher value of threshold voltage reduces the operation speed of a device. The proposed device has moderate value of threshold voltage as compared to its counterpart. It indicates improvement in

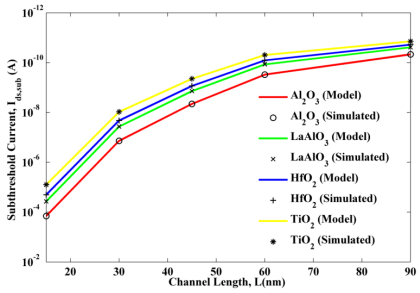

Fig. 6. Sub-threshold current of proposed device with various dielectric materials.

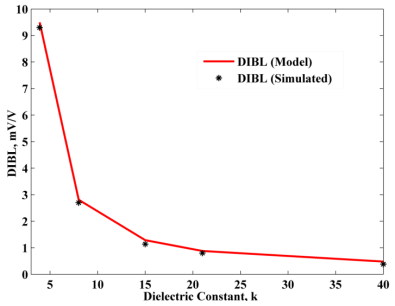

Fig. 7. DIBL effect of DH-DD-TM-SG MOSFET with various dielectric materials.

gate controllability due to channel engineering. Hence, proposed device is worthy for low power applications.

4. Sub-threshold Current

Fig. 6 depicts the sub-threshold current with various dielectric constant. The leakage current of device with $LaAlO_3$ as dielectric is $0.369X10^{-9}$ A. $ID_{,sub}$ of HfO_2 is $0.210X10^{-9}$ A, which indicate significant reduction in leakage current of 42.94% as compared to others. It is noticed from the Fig. 6 that leakage current reduces exponentially with increase in dielectric value. The high-κ materials provide more physical thickness which diminishes the tunneling of carriers through the insulator. So, proposed device with HfO_2 as dielectric significantly mitigates the leakage current which makes device suitable for low power applications.

5. DIBL Effect

A large bias at the drain causes DIBL in the MOSFET which degrade the device performance. The barrier height between source and channel becomes lowered [26]. Thus, control of gate terminal decreases over the channel. Fig. 7 illustrates the DIBL with varying dielectric constant. It is observed from the figure that SiO_2 has highest value of DIBL which is 9.49 mV/V. As the value of κ increases then corresponding exponentially decrement in DIBL are observed. HfO_2 reveals DIBL of 0.88 mV/V which points out significant reduction in DIBL. When DIBL of proposed device is compared with DIBL of Nirmal et al. [12] device it shows improvement of 26 %. Hence, proposed device provides better reduction of SCEs.

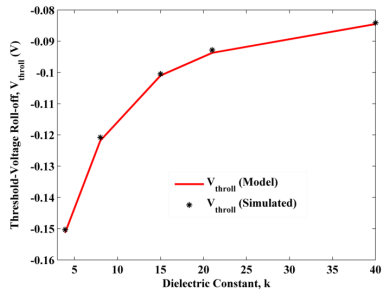

Fig. 8. Threshold voltage roll-off of DH-DD-TM-SG MOSFET with various dielectric materials.

6. Threshold Voltage Roll-off Effect

The attenuation of threshold voltage with attenuation in channel length is called "V_{th}-roll off" [27, 28]. Fig. 8 depicts the roll-off of threshold voltage. The V_{th}-roll off has been calculated by finding the deviation in threshold voltage for small and long channel devices. It is observed from the figure that SiO_2 has highest value of V_{throll} which is -0.15 V. As the value of κ increases then corresponding exponentially increase in V_{throll} are observed. HfO_2 reveals V_{throll} of -0.09 V which points out significant reduction in V_{throll}.

7. Sub-threshold Swing

SS is the minimum voltage required to enter into the ON state from the OFF state. The ideal value of SS is 60 mV/decade. Fig. 9 shows the SS as a function of variation in dielectric constant. SS decrease with increase in value of κ. It is observed from the figure that HfO_2 shows an improvement of 15.34% as compared to SiO_2 due to reduce leakage current in former oxide.

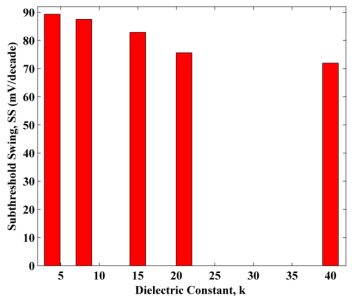

Fig. 9. Sub-threshold swing of proposed device with various dielectric materials.

IV. CONCLUSIONS

A 2D analytical model of proposed device has been presented for various gate dielectrics in terms of potential, field, and threshold voltage. This paper also described the various SCEs like DIBL, V_{throll} and SS. HfO_2 dielectric shows an excellent immunity against SCEs as compared to its counterpart. Potential and field exhibit extra peaks in their responses which is a clear sign of mitigation in HCEs. The improvement in DIBL, V_{throll} and SS are the direct consequences of gate stack and channel engineering. Leakage current is a key metric for standby power dissipation in device. HfO_2 exhibits very less leakage current as compared to SiO_2. Hence, proposed device is very useful for low power applications. In future, HfO_2 becomes the popular choice as a good insulator in the new generation devices.

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