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# Probabilistic based CMOS Adder for High Speed Communication Systems

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***Abstract*—Power efficient is an important availability for various mobile devices and communication system applications. The proposed probabilistic adder is to trade a lesser amount of accuracy with reduced power dissipation. In this paper, the probabilistic adder is eliminating the some part of the carry propagation path in least significant bit to reduce the power consumption and transistor count. The power consumption and probabilistic error behaviour of the proposed adder is designed and compared with other adders.**

***Index Terms*—Carry propagation path, communication systems, low power design, probabilistic approach, acceptable accuracy**

## I. INTRODUCTION

Adders are the basic blocks in different digital communication system applications such as modems, software defined radio, Dolby system and so on. In most of the communication system applications; human being can obtained valuable information from a little incorrect yield. The optimization of adders in terms of power, delay and transistor count has been presented in the literature [1].

The design of adder having low power consumption and low propagation delay results of great interest for the implementation of modern digital systems. Ripple carry and Manchester carry chain adders are the simplest, but slowest adders with O (n) area and O (n) delay, where *n* is an operand size. Carry look-ahead and parallel prefix adders have O (n log (n)) area and O (log (n)) delay to suffer by irregular layout. The critical path of Carry Save Adder (CSA) is either the ripple-carry path in the largest block or the worst case carry- select path.

The idea of an error tolerance and the PCMOS are important in digital communication subsystems [2]. The circuit is error tolerant if it contains faults that may cause both internal and external errors. The n-bit ETA-1 is splitting into m-blocks (m≥2). Each m blocks contain n/m bits of two separate parts such as sum and carry generator blocks. The dividing approach of this design depends on the total number of blocks. The chance of receiving an exact output becomes possible with longer delay path [3]. The design of an ETA-2 in [4, 5] is that operates by dividing the input into accurate MSB (Most Significant Bit) and inaccurate LSB parts. The modified ETA-2 is one of an imprecise adder based on RCA (Ripple Carry Adder). In this modified ETA-2 is dividing the carry propagation path into different slices of block. The error of this modified ETA-2 is limited by the length of MSB and bits per block.

The ways of improving chip yield by using imperfect chips in application where degradation of output quality is acceptable. The generation of acceptable results is more important than totally accurate results in digital application. The bio inspired adder is based on inexact logic whose truth table is to some extent different from the exact truth table of a full adder. Lower-part OR Adder (LOA) is split the n-bit addition into two parts such as l-bit and k-bit parts [6, 7]. In this LOA is not suitable for large input bit pattern. The error produced in this LOA is an increase as the number of increasing lower part length.

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The design of LOA is to avoid minor carry generated from the LSB with great loss of quality. The transistor level implementations of the AMAs (Approximate Mirror adders) are proposed in [8, 9] by reducing the number of different transistors. The design complexity is high for these approximate mirror adders with reasonable power consumption and accuracy.

The XOR/XNOR based adders [11] are implemented by pass transistor logic. These adders are consuming lot of power with less accuracy for larger bit width additions. Almost correct adder (ACA) is suitable for smaller bit width of the input with less probability of critical path propagation. This adder gives high probability of critical path for the large bit width of the input [11]. The implementation of probabilistic error tolerant adder is based on PCMOS for modeling the behavior of nano-metric design as well as reducing power consumption. The upper part of LSB values are suffered by accuracy problem for smaller as well as larger input bit width [12].

In a dubbed speculative adder circuit makes significant power than the traditional designs, but it consumes lot of area [13]. In structure [14], inverter gate is used to increase the circuit speed. In this circuit a large capacitive intermediate node will be created and this will increase the circuit power utilization.

A high performance and low voltage single bit full adder circuit [15] constructed with an internal logic which leads to has reduced PDP. It exhibit good driving capability and signal integrity for low voltage operation. The n-bit adder is constructed with this single bit full adder use high power and high transistor count. The approach is to examine the effect of device dissimilarities in ripple carry adder. The accuracy and reliability of the sum and carry output is complex processing for multi bit [16].

The proposed method is to simplify the hardness of a traditional adder by suppress the carry propagation path from LSB to MSB. In this paper the design difficulty of the traditional adder by reducing the number of gates and their connections. The design of high speed communication subsystems using this proposed CMOS adder blocks and estimate this adder blocks in terms of accuracy and power.

Any system that is not need to estimate the accurate LSB part of the sum, the proposed probabilistic CMOS adder has attain power, speed and transistor count by modifying the gate level implementation of LSB part of the adder. In Section II, present the proposed probabilistic CMOS adder for fast adder implementation. In Section III presents the design description of an adder. In section IV, to show the results and compare proposed probabilistic 32-bit CMOS adder with other adders. In Section V, is to give the conclusions.

## II. Proposed Design

The proposed probabilistic adder can split the n-bit addition process into two parts such as l-bit LSB and m-bit MSB. The LSB (Least Significant Bit) of an addition is estimated without consider the carry propagation. The MSB (Most Significant Bit) of an addition is estimated error free without consider the missing carry from the LSB part. The MSB of an adder is estimated error free and the LSB calculated by probabilistic logic. The proposed adder is reduced the design overhead by modifying the LSB of carry propagation path and reducing the crucial path.

The probabilistic adder consists of two blocks such as MSB part and LSB part. The multiplexer based ripple carry adder (RCA) is used for the MSB part of the probabilistic adder to achieve high speed and high precision. The LSB part is the most essential section in the proposed CMOS adder as it determines the power consumption, accuracy and transistor count of the adder. The LSB part is divided into LSB upper part and LSB lower part for carry free addition process.

## III. Design Description

### 1. Design of LSB Part

The LSB part consists of two parts such as LSB upper part and the LSB lower part. LSB lower part is constructed by several (l-2)-OR-gates and this gates are used to generate a sum bit ($S_0$-$S_{l-2}$)). The LSB upper part contains an additional NAND-AND gate is used to produce a sum ($S_{l-1}$) for upper part of the LSB and carry in ($C_{in}$) for MSB part. The carry generated from lower part LSB to upper part LSB of the adder to reduce its inaccuracy. The gate level implementation of MSB part and LSB part of the proposed adder is shown in Fig. 1.

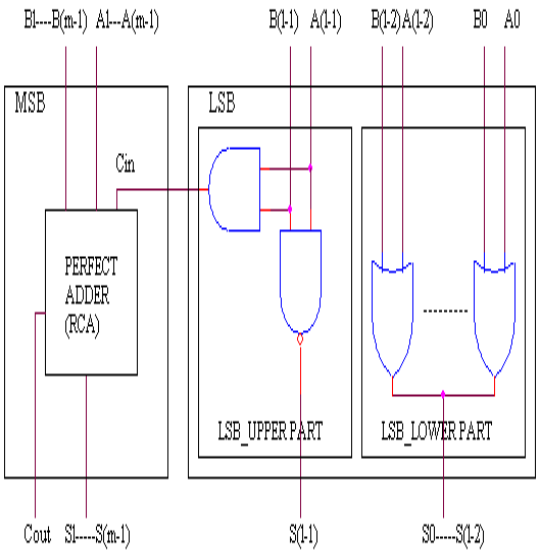


**Fig. 1.** The design of the proposed adder.

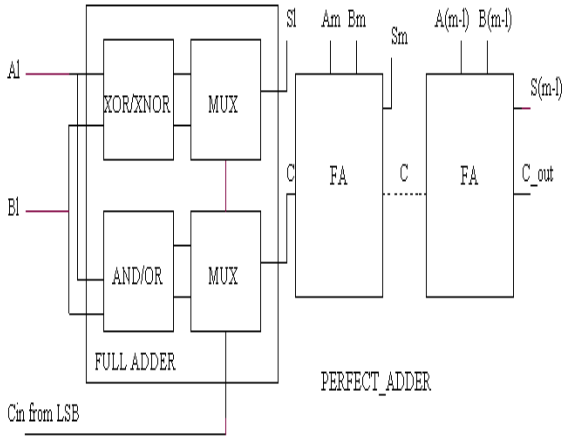


**Fig. 2.** Block diagram for MSB part of an adder.

## 2. Design of MSB Part

The MSB part of the perfect adder is constructed by using a multiplexer based full adder. The MSB part of the adder block is shown in Fig. 2. The two inputs such as Al & Bl of this MSB part are given in to full adder unit. At the same time the carry in (Cin) from the upper part of LSB is used as a selection signal for multiplexer based adder unit.

The carry output from every previous full adder block is used for selecting signal for the next multiplexer based full adder block and so on. This multiplexer based adder block is used to produce the individual sum output and final carry output for MSB part. The overall delay is determined by the MSB part, and also MSB part need be a fast adder. The given multiplexer in MSB part of an adder is constructed by using transmission gates where the number of transistors can be reduced.

**Table 1.** Truth Table for Full Adder

| A | B | C | Sum out | Carry out |
|---|---|---|---|---|
| 0 | 0 | **0** | 0 | 0 |
| 0 | 1 | **0** | 1 | 0 |
| 1 | 0 | **0** | 1 | 0 |
| 1 | 1 | **0** | 0 | 1 |
| 0 | 0 | **1** | 1 | 0 |
| 0 | 1 | **1** | 0 | 1 |
| 1 | 0 | **1** | 0 | 1 |
| 1 | 1 | **1** | 1 | 1 |

The truth table of full adder is shown in Table 1, it can be noticed that the sum output is equivalent to the A^B (AxorB) when C=0, and then equal to A~^B (AxnorB) when C=1. Similarly the carry output is equal to the A&B (AandB) when C=0, and A|B (AorB) when C=1. After this inspection a Mux (multiplexer) will be implemented to obtain the particular value established upon the carry input, as indicated earlier.

Hence, the power efficient method to design a mux based full adder for MSB part can be created by a MOS transistor unit to acquire the A~^B and A~^B signals, other MOS transistor unit to attain A&B and A|B signals, and two transmission gate based mux being run by the carry input to make the sum output and carry output as shown in Fig. 3. The advantages that can be expected for this power efficient mux based MSB part are there is no requirement of internal signal for controlling the select line of multiplexers. It reduces the capacitive load for the carry input, because it is connected only to some transistor gates and not to some source or drain terminals of the transistor.

This optimized proposed adder is constructed with partially Mux based design using Hardware Description Language (HDL). This proposed adder is incorporated in the traditional adder and its parameter comparison is made. so the proposed MSB part of probabilistic adder realized with AND/OR, XOR/XNOR and MUX is considered to be the greater performance adder circuit in terms of area, power and delay. It is observed that the proposed MSB part of probabilistic CMOS adder constructed with AND/OR, XOR/XNOR and MUX has attain low power, are and delay when compared to other combinations of the logic gate.

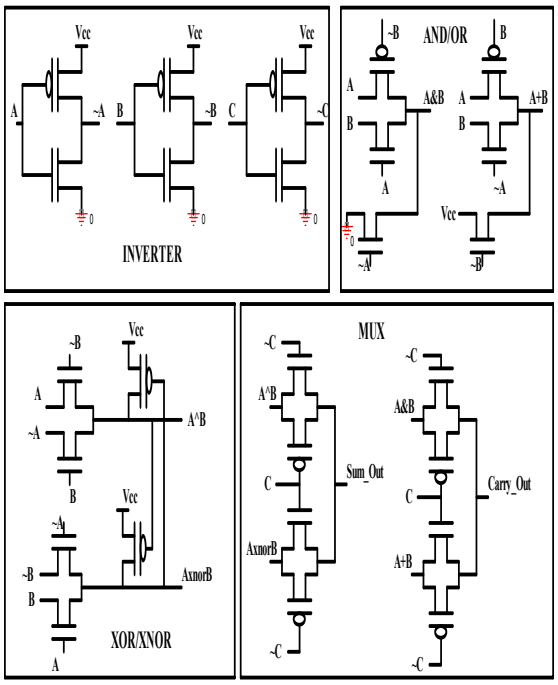


**Fig. 3.** Transistor based MSB part of an adder.

## 3. Power Consumption of an adder

The power consumption of an n-bit probabilistic adder is depends on the total number of gates are needed for an implementation. The single bit LSB lower parts are designed by one bit wise OR gate in place of five logic gates as used in other traditional adder.

The power consumption of LSB lower parts and LSB upper parts are

$$P_{LSB\_LOWER} = 0.2(l-1) \quad (1)$$

$$P_{LSB\_UPPER} = 0.4 \quad (2)$$

The total power consumption of LSB part is obtained from Eqs. (1) and (2) then

$$P_{LSB} = P_{LSB\_LOWER} + P_{LSB\_UPPER} \quad (3)$$

$$P_{LSB} = 0.2(l-1) + 0.4 \quad (4)$$

The total power consumption of the n-bit probabilistic adder is estimated by the sum of m-bit MSB part and l-bit LSB part.

$$P_{adder} = P_{LSB} + P_{MSB} \quad (5)$$

$$P_{adder} = m + 0.2(l-1) + 0.4 \quad (6)$$

**Table 2.** Power Consumption and Benefits of an Adder

| Design | Power Consumption (n-bit) | Power benefits (watts) |
|---|---|---|
| RCA | m+l | 0 |
| LOA | m+0.2l | 0.8l |
| AMA1 | m+0.85l | 0.15l |
| AMA2 | m+0.95l | 0.05l |
| AMA3 | m+0.8l | 0.2l |
| LIA | m+0 | l |
| PROPOSED | m+l (0.2+0.2/l) | 0.8l+0.8 |

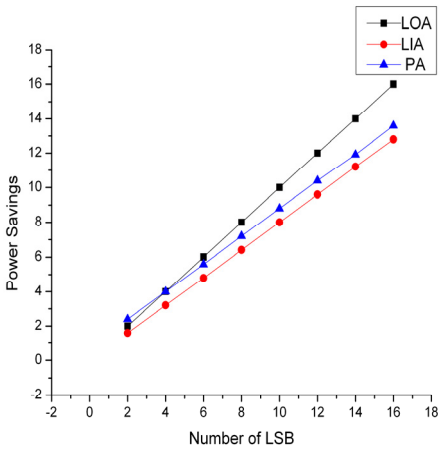


**Fig. 4.** Power Saving for the Proposed Adder.

$$P_{adder} = m + 0.2 * l + 0.2 \quad (7)$$

The power consumption and power benefit of different adders is shown in Table 2. The power savings for the LSB parts of different adder as shown in Fig. 4.

All the errors are exponentially varying with LSBs. The error changes are depends on the LSBs of an adder. The overall performance of probabilistic adder can be described with different computation such as Error (e), Mean error ($\bar{e}$) and Absolute mean error ($|\bar{e}|$).

The difference between the perfect result and imperfect result is called error function (e).

$$\text{Error(e)} = \text{Perfect result}(P_{ij}) - \text{Imperfect result}(P_{ij}) \quad (8)$$

The mean error is

$$\bar{e} = \frac{1}{(2^n-1)^2}\left[\sum_{i=0}^{2^n-1}\sum_{j=0}^{2^n-1}(P_{ij} - P'_{ij})\right] \quad (9)$$

where $P_{ij}$ and $P'_{ij}$ are perfect and imperfect results of an

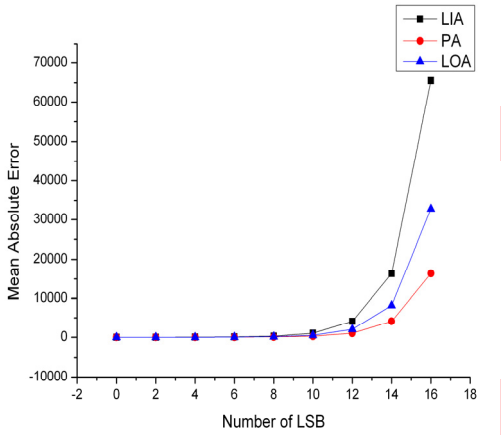


**Fig. 5.** Mean Absolute error for different adder.

**Table 3.** The error calculation for different adder

| Different Types of adder | Mean error | Absolute mean error | Absolute maximum error |
|---|---|---|---|
| LIA | $1\text{-}2^{LSB}$ | $2^{LSB}\text{-}1$ | $2^{LSB+1}\text{-}2$ |
| LOA | $1/4\text{-}2^{LSB-2}$ | $2^{LSB-2}\text{-}1/4$ | $2^{LSB}\text{-}1$ |
| PROPOSED | $1/2\text{-}2^{LSB-2}$ | $2^{LSB-2}\text{-}1/2$ | $2^{LSB-1}\text{-}2$ |

adder for different input pattern of n-bits. The mean values of multiple inputs are calculated by using mean absolute error. The mean absolute error is given by

$$\|\bar{e}\| = \frac{1}{(2^n-1)^2}\left[\sum_{i=0}^{2^n-1}\sum_{j=0}^{2^n-1}\left(\left|P_{ij}-P'_{ij}\right|\right)\right] \quad (10)$$

The mean absolute error for various adders as a function of different LSB is shown in Fig. 5. From the figure the proposed adder is better than that of other adder in terms of mean absolute error. The mean absolute error is reduced with the higher bit length of the adder. The aim of the proposed design is to minimize the power with sacrificing some reasonable accuracy.

Table 3 shows the error estimation of LIA (Lower part Ignored Adder), LOA (Lower part-OR-Adder) and the proposed PCA (Probabilistic CMOS Adder). LIA has to obtain maximum power benefits with high absolute mean error. LOA has the low power consumption and smaller delay; however, the transistor count is high. The probabilistic CMOS adder gives better performance in terms of power consumption, delay and transistor count with minimum absolute mean error.

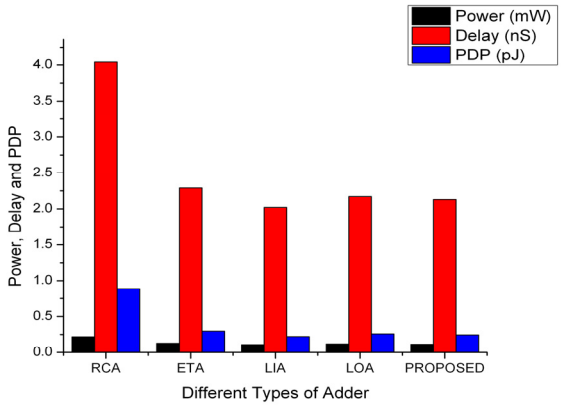


**Fig. 6.** Power and delay for different types of adder.

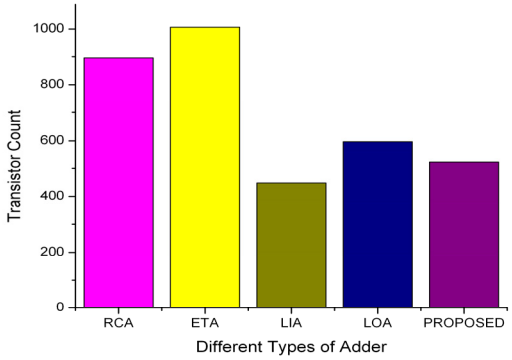


**Fig. 7.** Transistor count for different types of adder.

## IV. SIMULATION RESULTS

The proposed adder is designed and simulated using ISEsim. HSPICE software was used to construct the models of the 32-bit proposed and other adders. 1000 sets of inputs were randomly created using the MATLAB program. Designed for each position of input, on the way to run the simulation for each adder and recorded the power consumption. The transistor count was derived openly from the HSPICE software [6]. The power dissipation and delay of the 32 bit proposed and other adders are shown in Fig. 6. To compare the output of 32-bit proposed adder with actual value for 1000 number of samples, it is found that the average percentage of error is 1.5 i.e. the percentage of accuracy is 98.5%. Comparing the simulation and synthesis results of the proposed adder with those of other adders, it is evident that the proposed adder performed the best in terms of power consumption, delay and transistor count with less accuracy.

Fig. 7 denotes the total number of transistors present in

different adder circuits for 32 bit addition process. This shows that the traditional ripple carry adder (RCA) and error tolerant adder (ETA) has permitting the highest number of transistors (more than 900 transistors) for the implementation of 32 bit adder circuit. But, the proposed probabilistic adder is allowing the minimum number of transistor (less than 500 transistors) for implementation of 32-bit adder circuit. By way of the number of transistor decreases, complexity of the proposed adder will be diminished, which in turn reduces the transistor counts. This is extremely useful in new CMOS technology. From the Fig. 7, it is very clear that the proposed probabilistic CMOS adder has less transistor count compare with other type of adders.

## V. CONCLUSIONS

The probabilistic adder is to provide a physically compact with low power consumption. The core part of communication subsystem, this adders are in extremely high efficient on its speed and area. To reduce major power consumption of an adder design it is a good direction to reduce number of gates thereby reducing a dynamic power which is a major part of total power dissipation. The proposed probabilistic CMOS adder described in this paper provides further discernment and greater understanding of establishing part of the communication subsystems to benefit the designers in building their selections. Simulation results illustrate the superiority of the resulting proposed adder against conventional adders in terms of power, delay and area. The simulation and analysis on large proposed adder blocks maintained an acceptable accuracy while offering benefits on power. The proposed adder is mostly applicable to high speed communication subsystems.

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