JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.21, NO.2, APRIL, 2021
https://doi.org/10.5573/JSTS.2021.21.2.092
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Erase Speed Enhancement with Low Power Operation by Incorporating Boron Doping

Young Suh Song[1,2], Taejin Jang[2], Hyun-Min Kim[2], Jong-Ho Lee[2], and Byung-Gook Park[2,*]

***Abstract*—In this paper, it is shown that the erase efficiency of the Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) type nonvolatile charge trapping memory (CTM) is greatly improved by adjusting boron doping. Tunnel FET (TFET) based SONOS memory, which has p-type at source side, is superior to MOSFET based SONOS memory in terms of hole supplement and erase speed. In order to discover the specific physical reasons of this erase speed enhancement, MOSFET based SONOS memory devices with different body doping concentration are additionally investigated. As a result, it is found that the more hole supplement from source side in TFET and body side in MOSFET accelerates the erase speed and erase speed enhancement can be realized by utilizing boron doping. Furthermore, erase speed depending on device geometry, in terms of source-to-gate overlap length and gate length, is also analyzed. Interestingly, it is demonstrated that source overlap technique, which has been implemented for suppression of ambipolar current, is also possible to accelerate erase speed.**

***Index Terms*—SONOS memory, tunnel FET (TFET), erase speed, erase efficiency, nonvolatile charge trapping memory (CTM)**

Manuscript received Mar. 24, 2020; reviewed Dec. 20, 2020; accepted Mar. 18, 2021
[1]Department of Computer Science, Korea Military Academy (KMA), Seoul 01805, Korea
[2]Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, Korea
E-mail : bgpark@snu.ac.kr

I. INTRODUCTION

As the growth of big data market and the demand for increased volume of the stored data increases, Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) nonvolatile charge trapping memories (CTM) have been widely studied due to higher endurance, better scalability, and lower power consumption compared to the conventional floating gate memories [1-6]. However, even though this SONOS structure has been broadly adopted and investigated in flash technology, the program and erase speed (P/E) is still one of the main issues needed to be improved. Specifically, when the tunneling oxide thickness becomes thinner for fast P/E operation, the increased direct tunneling leads to significant charge loss and finally results in degradation of retention characteristics. In order to solve this problem, several approaches on gate stacks have been proposed, such as bandgap engineered (BE) tunneling oxide [7, 8], high-*k* dielectrics and metal gate [9, 10], BE charge trapping layer (CTL) [11], and in-situ silicon nanocrystals embedded in Si_3N_4 CTL [6]. However, these proposed techniques in previous researches with controlling the oxide thickness concomitantly face with trade off issues such as relationship between P/E speed enhancement from thinner thickness and retention degradation [12, 13].

More importantly, since the hole barrier between Si and SiO_2 (4.7 eV) is higher than the electron barrier (3.2 eV) between them during P/E operation [14-17], the erase speed is one of the main challenge of SONOS memory needed to be overcome [18-22]. Even though this issue can be improved by applying higher erase voltage, this solution results in higher power consumption.

Therefore, another 'intrinsic' solution is still needed to improve erase speed. Considering the erase speed is mainly determined by the movement of hole, it can be intrinsic solution to manipulate the p-type doping concentration. Specifically, Tunnel FET (TFET), which has been widely researched for low power operation, have numerous p-type dopant in source side. Since TFET has about 100,000 times of hole concentration in source side compared to metal-oxide-semiconductor field-effect-transistors (MOSFET), it is surmised that the TFET based memory structure can remarkably improve the erase speed of memory device. Even though this doping technique can be a viable solution for erase speed enhancement, the approach on doping technique hasn't been widely studied for improving erase speed.

In this work, the aim of this paper is to improve erase speed without making tunneling oxide thinner, by utilizing the structure of TFET. Erase speed enhancement by boron (B) doping is proposed and investigated in this paper. The relationship between B doping and erase efficiency is investigated through memory devices based on MOSFET and TFET structures.

This paper is organized as follows. First, the basic program and erase characteristics such as change in electron trapped charge density and hole trapped charge density are analyzed. Then, the improvement of erase efficiency from the TFET structure have been widely investigated with erase speed, change of threshold voltage, and the cross-sectional illustration describing the increased hole supplement. Finally, the effect of gate length (L_{gate}) and source-to-gate overlap length ($L_{Source\ overlap}$) on erase speed have been additionally analyzed for more detail investigation.

II. Device Structure and Model Physics

Cross-sectional views of MOSFET based SONOS and TFET based SONOS are schematically shown in Fig. 1. As SOI SONOS devices [23-25], the devices in this work have gate, source and drain terminals, and no body terminal in order to reduce fabrication cost. Table 1 describes the film thickness and channel length for these devices. The blocking oxide and tunneling oxide are composed of SiO_2 films and their thickness is 9 nm and 3 nm, respectively. The charge trapping layer is composed of 6 nm thick Si_3N_4. In both types of devices, the channel

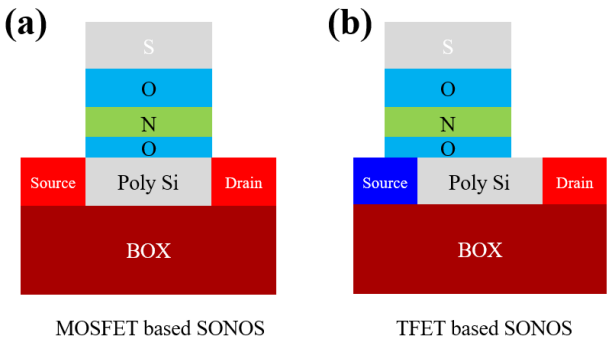

Fig. 1. Schematic view illustrating (a) MOSFET based SONOS memory, (b) TFET based SONOS memory.

Table 1. Film thickness and channel length in SONOS devices based on MOSFET and TFET structures

	Material	Thickness [nm]
Blocking oxide	SiO_2	9
Charge trapping layer	Si_3N_4	6
Tunneling oxide	SiO_2	3
Channel thickness	Si	12
Channel length	Si	60

length is 60 nm. The n^+ source/drain and p body in MOSFET based SONOS device have doping concentrations of 1×10^{20} cm^{-3} and 1×10^{15} cm^{-3}, respectively. In TFET based SONOS device, which is suitable for low power operation, the p^+ source and n^+ drain have a doping concentration of 1×10^{20} cm^{-3}, respectively, and the p region of channel has a doping concentration of 1×10^{15} cm^{-3} [26, 27]. A drain-to-gate underlap (source-to-gate overlap) structure is applied to the TFET to suppress the ambipolar current, which undesirably increases the off state current.

In order to investigate the electrical characteristics of these two devices, physical models such as band-to-band tunneling (BTBT), trap-assisted-tunneling (TAT), Shockley-Read-Hall (SRH) recombination, and electric field saturation models are applied in the device simulation using Synopsys Sentaurus™ TCAD tool. Furthermore, for the purpose of modeling Si_3N_4 as CTL, charge trap density of 3×10^{19} cm^{-3} is applied for Si_3N_4 which corresponds to charge trap density of Si_3N_4 in SONOS device [28], and nonlocal mesh was also used for adjusting Fowler-Nordheim (FN) tunneling and direct tunneling.

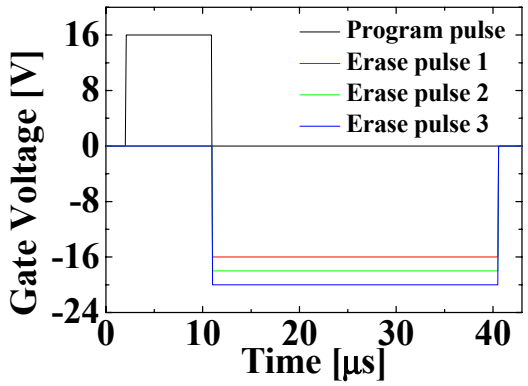

Fig. 2. Program and erase pulse scheme.

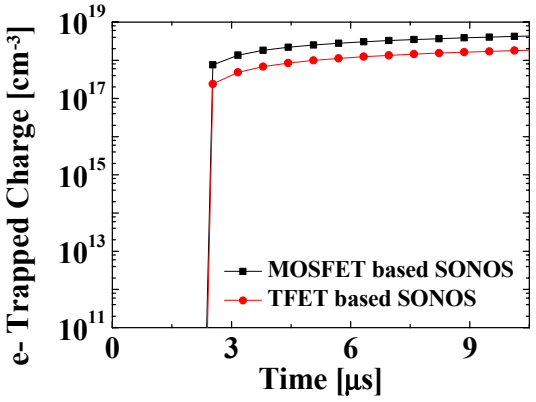

Fig. 3. Electron trapped charge density change during program operation.

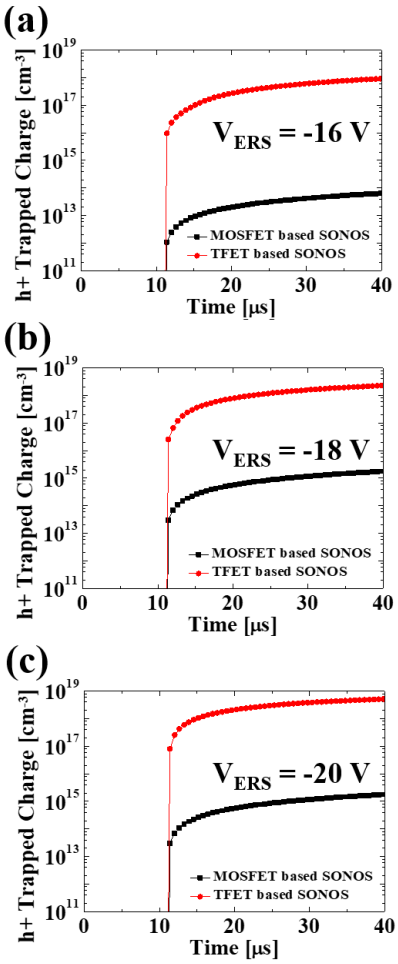

Fig. 4. Hole trapped charge density change during erase operation with erase voltages of (a) -16 V, (b) -18 V, (c) -20 V.

III. Demonstration of Erase Speed Enhancement

As illustrated in Fig. 2, the program voltage of 16 V and erase voltages of -16, -18, -20 V were applied to gate for investigating the effect of doping concentration on the P/E speed. Fig. 3 and 4 illustrates the program and erase efficiency respectively by comparing MOSFET based SONOS and TFET based SONOS.

Even though TFET based SONOS has 3 times lower programing efficiency compared to MOSFET based SONOS, TFET based SONOS has 10^4 times higher erase efficiency as shown in Fig. 3 and 4. Specifically, a slight degradation of program can be explained by drain underlap and the dopant distribution. Since MOSFET based SONOS has n-type dopant in both source and drain region while TFET based SONOS has n-type dopant only in the drain region (which is located far away from charge trapping layer in the underlap structure), MOSFET based SONOS has slightly higher program efficiency compared to TFET based SONOS. In the same vein, the erase speed enhancement can be also explained by the dopant distribution. Since TFET based SONOS has a p-type doping concentration of 1×10^{20} cm^{-3} in the source region and whereas MOSFET based SONOS hasn't, the TFET based SONOS is significantly superior to MOSFET based SONOS in erase speed. Furthermore, this erase speed enhancement can be achieved for various erase voltages such as -16 V, -18 V, and -20 V as shown in Fig. 4.

The transfer characteristics before and after erase operation was demonstrated in Fig. 5. For the fair comparison, threshold voltage was calculated when drain current is 10^{-8} A/μm for MOSFET based SONOS and 10^{-10} A/μm for TFET based SONOS, because TFET derives low current and the new threshold voltage is needed to be defined [29]. TFET based SONOS device showed threshold voltage shift about 0.61 V and this value is

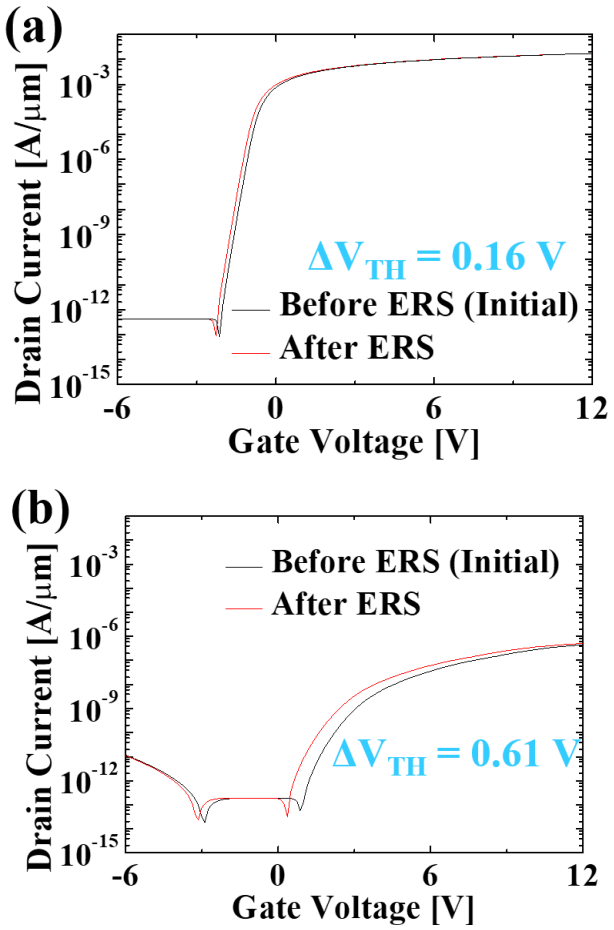

Fig. 5. Transfer characteristics before and after erase operation by V_{ERS} = -20 V with (a) MOSFET based SONOS, (b) TFET based SONOS.

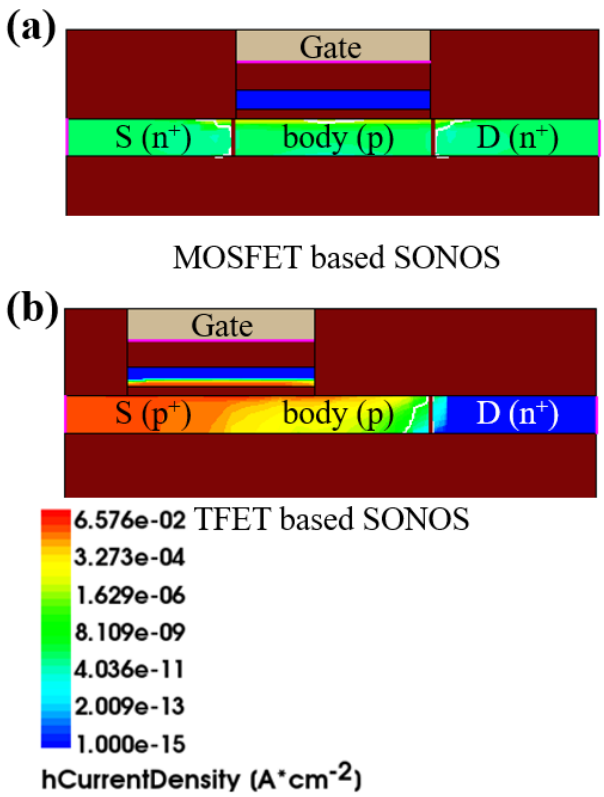

Fig. 6. Hole current density during erase operation by V_{ERS} = -20 V with the cross-sectional view of (a) MOSFET based SONOS, (b) TFET based SONOS.

about 4 times of MOSFET based SONOS device. In addition, TFET based SONOS has additional advantage of lower off current and lower on current, which is suitable for low power application, as shown in Fig. 5.

In summary, since p/i/n structure of TFET based SONOS is possible to supply significant amount of hole from source, erase speed can be significantly improved about 10^4 times with the advantage of low power operation for low power NAND flash application and low power NOR flash application.

IV. Additional Physical Analyzation on Erase Speed Enhancement

In order to investigate the physical mechanism of erase speed improvement, hole current density during erase operation is investigated with MOSFET based SONOS and TFET based SONOS. As shown in Fig. 6, TFET based SONOS has about 10^6 times of hole current density compared to MOSFET based SONOS. Since TFET based SONOS can receive numerous amount of hole from p-type source, significant hole current can flow at the channel of TFET based SONOS. In addition, TFET based SONOS is possible to derive both of significant electron current from n-type drain and enormous hole current from p-type source, and this advantage is very crucial to TFET based memory application. Therefore, the doping technique is very strategic to memory operation.

Moreover, the relationship between erase efficiency and body doping concentration of MOSFET based SONOS device is also investigated to discover the specific reason of erase speed enhancement as shown in Fig. 7. For all cases with erase voltage of -16, -18, -20 V, MOSFET with higher body doping concentration has higher erase efficiency. In particular, erase efficiency is significantly improved when the body doping concentration becomes bigger than 5×10^{19} cm^{-3}. This is because when the body doping concentration becomes

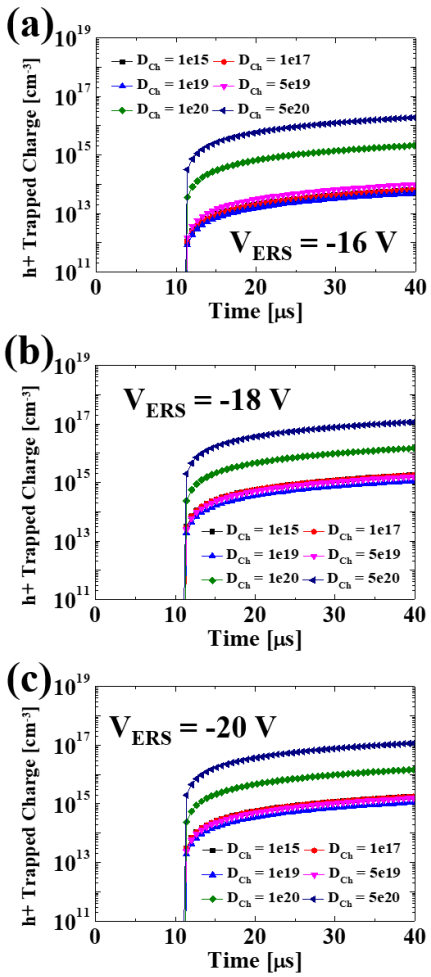

Fig. 7. Relationship between erase efficiency and body doping of MOSFET based SONOS device with erase voltage of (a) -16 V, (b) -18 V, (c) -20 V.

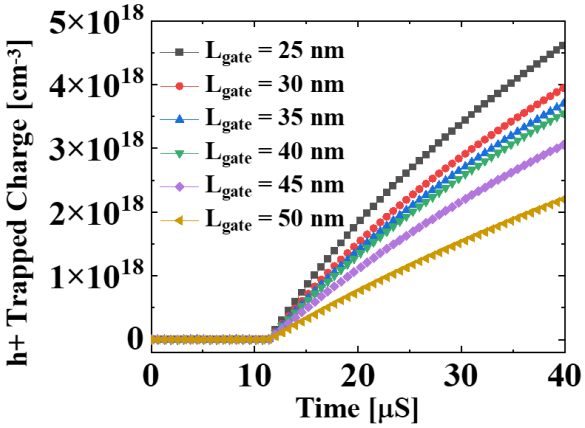

Fig. 8. Analysis on the effect of gate length on the erase speed in TFET based SONOS.

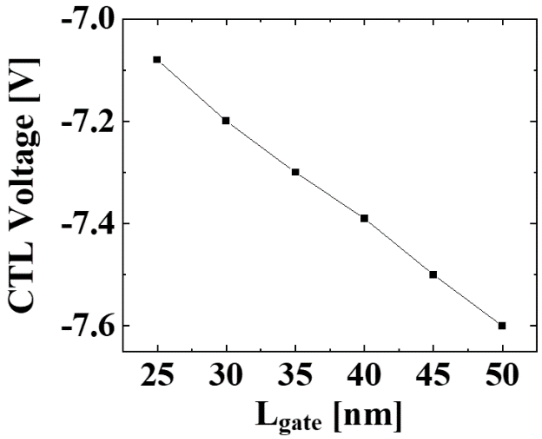

Fig. 9. Effect of scaling on the potential of CTL in TFET based SONOS during erase operation.

bigger than 5×10^{19} cm^{-3}, not only more hole supplement occurs, but also bandgap narrowing of silicon channel [30] also helps more hole movement. Specifically, when the bandgap narrowing occurs [30], the bandgap of silicon becomes narrower and energy of conduction band decreases. Therefore, the hole in the conduction band of channel easily moves to charge trap layer (CTL), and the erase speed is greatly improved when the body doping concentration becomes greater than 5×10^{19} [Fig. 7]. Therefore, our aforementioned analysis 'The erase speed improvement at TFET based SONOS originates from considerable amount of hole supplement from source can be a reasonable analyzation.

Furthermore, this erase speed improvement achieved by increased body doping can apply in three-dimensional (3D) vertical NAND (VNAND) application. By adjusting the doping concentration of channel, it is expected that the 3D VNAND structure is also possible to improve erase efficiency. In particular, erase speed of the cells which are not located in the edge of VNAND string can be effectively improved by this doping technique.

Regarding the scaling issues, it has been demonstrated that the scaling of memory devices deteriorates the erase speed efficiency [Fig. 8]. This can be explained by the relationship between scaling and gate controllability. From the previous research [31], it is well known fact that the scaling with short L_{gate} decreases gate controllability. Namely, the decreased gate controllability from short L_{gate} deteriorates the potential of CTL during erase operation [Fig. 9], and therefore the erase speed of scaled memory device becomes worse [Fig. 8].

Regarding device geometry of source-to-gate overlap

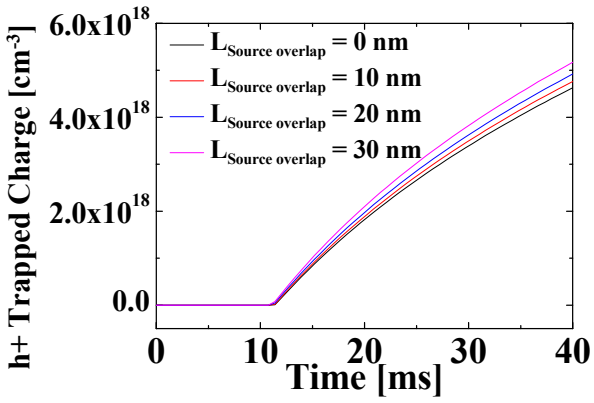

Fig. 10. Analysis of erase speed enhancement depending device geometry of TFET (Source overlap length ($L_{Source\ overlap}$) will be illustrated in Fig. 12).

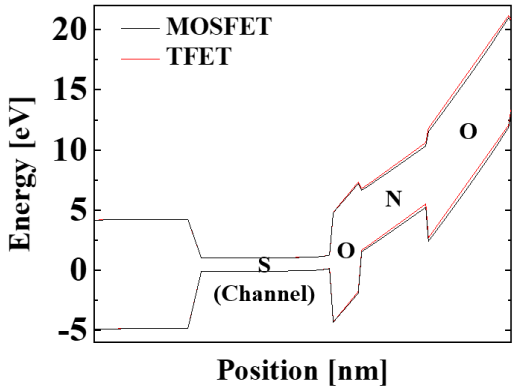

Fig. 11. Comparison of energy band diagram of MOSFET based SONOS (black line) and that of TFET based SONOS (red line) during erasing operation. The abbreviated letters S, O, N, O stand for Si (channel), SiO_2 (tunneling oxide), Si_3N_4 (CTL), SiO2 (blocking oxide) respectively.

in TFET, which has been widely investigated for the suppression of ambipolar current [32, 33], erase speed is slightly increased as $L_{Source\ overlap}$ increases [Fig. 10]. Since source side in TFET has higher hole current density as demonstrated in Fig. 6(b), the TFET device with higher $L_{Source\ overlap}$ has higher erase efficiency. In addition, the energy band diagram during erase operation [Fig. 11] also demonstrates that the TFET has higher erase efficiency and stores more amount of hole during erase operation.

Even though the increase of erase speed from source overlap (1.12 times) is somewhat small compared to that from boron doping technique at source region (10^4 times), it is remarkable that the source overlap can improve not only ambipolar current [32, 33] but also erase speed at the same time.

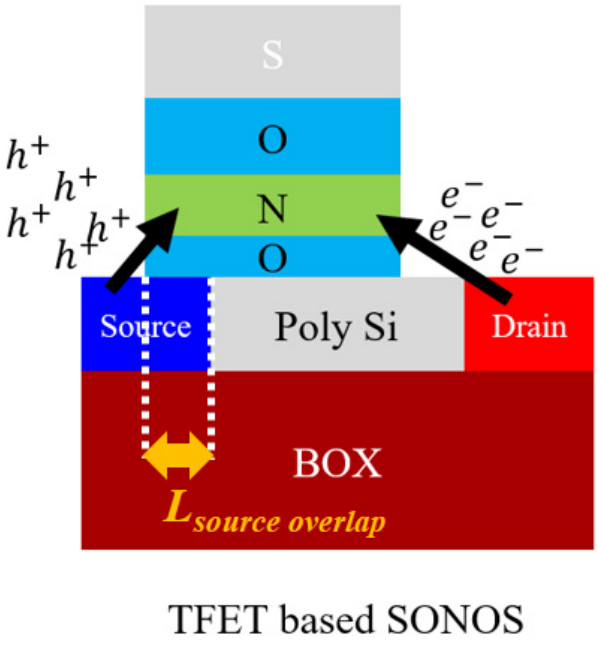

Fig. 12. Schematic diagram illustrating both of hole supplement (source) and electron supplement (drain) in TFET based SONOS.

In summary, the erase speed enhancement by incorporating TFET structure is achieved by the asymmetric structure of TFET, namely structure with electron supplier of n^+ type drain and hole supplier of p^+ type source [Fig. 12]. Therefore, TFET can be a viable solution for the future memory device with enhanced erase speed and source overlap in TFET can contribute to not only suppression of ambiploar current but also enhancement of erase speed as well.

V. Conclusions

In this paper, we have demonstrated erase speed enhancement at Tunnel FET (TFET) based SONOS device. From the several analyzation on physical mechanism of erase speed enhancement, it has been demonstrated that this erase speed enhancement originates from significant amount of hole supplement through p-type source. Even though TFET based SONOS has 3 times lower programing efficiency compared to MOSFET based SONOS, TFET based SONOS has 10^4 times higher erase efficiency in terms of trapped charge. In addition, the transfer curve showed the threshold voltage shift with TFET based SONOS is about 4 times compared to threshold shift with MOSFET based

SONOS. In essential, TFET based SONOS is possible to flow both of significant electron current from n^+ drain and enormous hole current from p^+ source, and this advantage is very strategic to memory application. Therefore, the doping technique is very important in operation of memory devices and TFET based memory can be a promising candidate for the future low power application with higher erase speed.

ACKNOWLEDGMENTS

This work was supported by 2021 research fund of Korea Military Academy (Hwarangdae Research Institute). This work was supported in part by the Brain Korea 21 Plus Project in 2021.

REFERENCES

[1] Y. Liu, et al., "Electric Field Induced Nitride Trapped Charge Lateral Migration in a SONOS Flash Memory," *IEEE Electron Device Letters*, Vol. 38, No. 1, pp. 48-51, Jan. 2017.

[2] E. R. Hsieh, H. T. Wang, S. S. Chung, W. Chang, S. D. Wang and C. H. Chen, "Experimental techniques on the understanding of the charge loss in a SONOS nitride-storage nonvolatile memory," *2016 IEEE 23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, pp. 38-42, July 2016.

[3] D. Gupta and S. K. Vishvakarma, "Impact of LDD Depth Variations on the Performance Characteristics of SONOS NAND Flash Device," *IEEE Transactions on Device and Materials Reliability*, Vol. 16, No. 3, pp. 298-303, Sep. 2016.

[4] J. -W. Jung and W. -J. Cho, "Tunnel Barrier Engineering for Non-Volatile Memory," *Journal of Semiconductor Technology and Science*, Vol. 8, No. 1, pp. 32-39, Mar. 2008.

[5] T. Kim, K. Park, T. Jang, M. H. Baek, Y. S. Song and B. -G. Park, "Input-modulating adaptive neuron circuit employing asymmetric floating-gate MOSFET with two independent control gates," *Solid-State Electronics*, Vol. 163, pp. 107667-1-107667-5, Jan. 2020.

[6] T. Kim, Y. S. Song and B. -G. Park, "Overflow handling integrate-and-fire silicon-on-insulator neuron circuit incorporating a Schmitt trigger implemented by back-gate effect," Vol. 19, No. 10, pp. 6183-6186, Oct. 2019.

[7] H. -T. Lue, et al, "BE-SONOS: A bandgap engineered SONOS with excellent performance and reliability," *IEEE International Electron Devices Meeting*, pp. 547-550, Dec. 2005.

[8] Y. S. Song, et al., "Tunneling oxide engineering for improving retention in nonvolatile charge-trapping memory with TAHOAOS (TaN/Al2O3/HfO2/SiO2/Al2O3/SiO2/Si) structure," *Japanese Journal of Applied Physics*, Vol. 59, No. 6, pp. 061006-1-061006-7, June 2020.

[9] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park and K. Kim, "A novel SONOS structure of SiO/sub 2//SiN/Al/sub 2/O/sub 3/ with TaN metal gate for multi-giga bit flash memories," *IEEE International Electron Devices Meeting*, pp. 26.5.1-26.5.4, Dec. 2003.

[10] Y. Choi, et al., "Simulation of the effect of parasitic channel height on characteristics of stacked gate-all-around nanosheet FET," *Solid-State Electronics*, Vol. 164, pp. 107686-1-107686-7, Feb. 2020.

[11] K. -H. Wu, H. -C. Chien, C. -C. Chan, T. -S. Chen and C. -H. Kao, "SONOS device with tapered bandgap nitride layer," *IEEE Transactions on Electron Devices*, Vol. 52, No. 5, pp. 987-992, May 2005.

[12] W. Guan, S. Long, M. Liu, Q. Liu, Z. Li, and R. Jia, "Modeling of retention characteristics for metal and semiconductor nanocrystal memories," *Solid-State Electronics*, Vol.51, No.5, pp. 806-811, May 2007.

[13] Y. Liu, S. Tang, and S. K. Banerjee, "Tunnel oxide thickness dependence of activation energy for retention time in SiGe quantum dot flash memory," *Applied Physics Letters*, Vol.88, pp. 213504-1-213504-3, Jan. 2006.

[14] S. Choi, J. Han, S. Kim, D. Moon, M. Jang and Y. Choi, "A novel TFT with a laterally engineered bandgap for of 3D logic and flash memory," *Symposium on VLSI Technology*, pp. 111-112, June 2010.

[15] S. Wang, et al, "Reliability and Processing Effects of Bandgap Engineered SONOS (BE-SONOS) Flash Memory," *IEEE International Reliability Physics Symposium Proceedings*, pp. 171-176, April 2007.

[16] Y. S. Song, J. H. Kim, G. Kim, H. -M. Kim, S. Kim and B. -G. Park, "Improvement in Self-heating Characteristic by Incorporating Hetero-gate-dielectric in Gate-All-Around MOSFETs," *IEEE Journal of the Electron Devices Society*, doi: 10.1109/JEDS.2020.3038391.

[17] Y. S. Song, et al., "Improvement in Self-Heating Characteristic by Utilizing Sapphire Substrate in Omega-Gate-Shaped Nanowire Field Effect Transistor for Wearable, Military, and Aerospace Application," *Journal of Nanoscience and Nanotechnology*, Vol. 21, No. 5, pp. 3092-3098, May 2021. https://doi.org/10.1166/jnn.2021.19149

[18] R. Lo, et al., "A Study of Blocking and Tunnel Oxide Engineering on Double-Trapping (DT) BE-SONOS Performance," *IEEE International Memory Workshop (IMW)*, pp. 1-4, May 2015.

[19] M. R. Zakaria, S. R. Kasjoo, A. F. Mahyidin, A. W. Al-Mufti, R. M. Ayub and U. Hashim, "Fabrication of SONOS flash memory device by using engineered tunnel barrier technique," *IEEE International Conference on Semiconductor Electronics (ICSE2014)*, pp. 436-439, Aug. 2014.

[20] A. Padovani, et al., "A Comprehensive Understanding of the Erase of TANOS Memories Through Charge Separation Experiments and Simulations," *IEEE Transactions on Electron Devices*, Vol. 58, No. 9, pp. 3147-3155, Sept. 2011.

[21] A. Mauri, et al., "A new physics-based model for TANOS memories program/erase," *IEEE International Electron Devices Meeting*, pp. 1-4, Dec. 2008.

[22] Y. Park, et al., "Highly Manufacturable 32Gb Multi -- Level NAND Flash Memory with 0.0098 μm2 Cell Size using TANOS(Si - Oxide - Al2O3 - TaN) Cell Technology," *International Electron Devices Meeting*, pp. 1-4. Dec. 2006.

[23] A. Padilla, and T. K. Liu, "Dual-bit SONOS FinFET Non-Volatile Memory Cell and New Method of Charge Detection," *2007 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, pp. 1-2, Apr. 2007.

[24] P. Xuan, M. She, B. Harteneck, A. Liddle, J. Bokor and T. -. King, "FinFET SONOS flash memory for embedded applications," *IEEE International Electron Devices Meeting 2003*, pp. 26.4.1-26.4.4, Dec. 2003

[25] I. Fujiwara, H. Aozasa, A. Nakamura, Y. Hayashi, and T. Kobayashi, "MONOS memory cell scalable to 0.1um and beyond," *IEEE Non-Volatile Semiconductor Memory Workshop*, pp. 117-118, 2000.

[26] C. Anghel, Hraziia, A. Gupta, A. Amara, and A. Vladimirescu, "30-nm Tunnel FET With Improved Performance and Reduced Ambipolar Current," *IEEE Transactions on Electron Devices*, Vol. 58, No. 6, pp. 1649-1654, June 2011.

[27] G. Leung, and C. O. Chui, "Stochastic Variability in Silicon Double-Gate Lateral Tunnel Field-Effect Transistors," *IEEE Transactions on Electron Devices*, Vol. 60, No. 1, pp. 84-91, Jan. 2013.

[28] X. Zou, et al, "The influence of grain boundary interface traps on electrical characteristics of top select gate transistor in 3D NAND flash memory," *Solid-State Electronics*, Vol. 153, pp. 67-73, Mar. 2019.

[29] K. Boucart, and A. M. Lonescu, "A new definition of threshold voltage in Tunnel FETs," *Solid-State Electronics*, Vol. 52, No. 9, pp. 1318-1323, Sep. 2008.

[30] H. P. D. Lanyon, et al., "Bandgap narrowing in moderately to heavily doped silicon," *IEEE Transactions on Electron Devices*, Vol. 26, No. 7, pp. 1014-1018, July 1979.

[31] M. -D. Ko, et al., "Study on a Scaling Length Model for Tapered Tri-Gate FinFET Based on 3-D Simulation and Analytical Analysis," *IEEE Transactions on Electron Devices*, Vol. 60, No. 9, pp. 2721-2727, July 2013.

[32] R. Goswami, et al., "Hetero-gate-dielectric gate-drain underlap nanoscale TFET with a δp^+ Si1-xGex layer at source-channel tunnel junction," *2014 International Conference on Green Computing Communication and Electrical Engineering*, Mar. 2014.

[33] J. H. Kim, et al., "Analysis of Current Variation with Work Function Variation in L-Shaped Tunnel-Field Effect Transistor," *Micromachines*, Vol. 11, No. 8, pp. 780-789, Aug. 2020.

Young Suh Song is Professor in department of Computer Science (CS) at Korea Military Academy. His current research interests have included semiconductor reliability (self-heating effect and retention characteristics), AI semiconductor, Machine Learning (ML) for demographics and economics, NAND Flash and NOR Flash, low temperature logic device for CPU, low power logic device (Tunnel FET, TFET) for cell phone and laptop, and germanium (Ge) based logic device (2030 ~ 2050) which is one of the promising candidates for replacing current silicon (Si) based CPU technology. He has authored and co-authored over 30 research papers in journals and conferences. He served as a member on several international conferences including International Microprocesses and Nanotechnology Conference (MNC), International Nanotech Symposium & Exhibition, and Institute of Electrical and Electronics Engineers (IEEE). He received "Best Paper" Award from the Institute of Electronics and Information Engineers (IEIE) in 2021.

Taejin Jang received the B.S degrees in the Department of Electrical and Computer Engineering from Seoul National University, Seoul, Korea, in 2016. He is currently in MS & PhD course in the Department of Electrical and Computer Engineering at Seoul National University. His recent interests include SB Schottky Barrier MOSFET, synaptic devices, AND flash, NOR flash, and neuromorphic system.

Hyun-Min Kim received the B.S degrees in the Department of Electrical and Computer Engineering from Seoul National University, Seoul, Korea, in 2016. He is currently in MS & PhD course in the Department of Electrical and Computer Engineering at Seoul National University. His recent interests include Tunnel FET, low power operation, Thin Film Transistor, CMOS technology.

Jong-Ho Lee received the B.S. degree from Kyungpook National University, Daegu, Korea, in 1987 and the M.S. and Ph.D. degrees from Seoul National University, Seoul, in 1989 and 1993, respectively, all in electronic engineering. In 1993, he worked on advanced BiCMOS process development at ISRC, Seoul National University as an Engineer. In 1994, he was with the School of Electrical Engineering, Wonkwang University, Iksan, Chonpuk, Korea. In 2002, he moved to Kyungpook National University, Daegu Korea, as a Professor of the School of Electrical Engineering and Computer Science. Since September 2009, he has been a Professor in the School of Electrical and Computer Engineering, Seoul National University, Seoul Korea.

Byung-Gook Park received his B.S. and M.S. degrees in electronics engineering from Seoul National University (SNU) in 1982 and 1984, respectively, and his Ph. D. degree in electrical engineering from Stanford University in 1990. From 1990 to 1993, he worked at the AT&T Bell Laboratories, where he contributed to the development of 0.1 micron CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, developing 0.25 micron CMOS. In 1994, he joined SNU as an assistant professor in the School of Electrical Engineering (SoEE), where he is currently a professor. His current research interests include the design and fabrication of nanoscale CMOS, flash memories, silicon quantum devices and organic thin film transistors. He has authored and co-authored over 1000 research papers in journals and conferences. Prof. Park has served as a committee member on several international conferences including Microprocesses and Nanotechnology, IEEE International Electron Devices Meeting, International Conference on Solid State Devices and Materials, and IEEE Silicon Nanoelectronics Workshop and served as an Editor of IEEE Electron Device Letters.