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# Silicon-controlled Rectifier-based Electrostatic Discharge Protection Circuit with Additional NPN Parasitic Bipolar Junction Transistor for 5-V Application

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*Abstract*—**This paper proposes a novel protection circuit based on a silicon-controlled rectifier (SCR) to prevent electrostatic discharge (ESD) at low voltages. The proposed device consists of an additional NPN parasitic bipolar transistor operated via application of an N+ diffusion region and a well breakdown voltage, to reduce the high trigger voltage caused by the well breakdown voltage of the existing SCR structure. Furthermore, the proposed device exhibits an improved trigger voltage, holding voltage, and dynamic resistance component when compared with existing parasitic PNP bipolar transistors. The proposed ESD protection circuit was manufactured using a 0.18 μm bipolar-CMOS-DMOS; it exhibited a significant improvement in electrical characteristics such as trigger voltage (8.1 V) and holding voltage (3.55 V), according to the results of transmission line pulse measurement. Hence, it is deemed to be suitable for 5-V-class applications.**

*Index Terms*—**Electrostatic discharge (ESD), ESD clamp, silicon-controlled rectifier (SCR), holding voltage, trigger voltage**

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## I. INTRODUCTION

Electrostatic discharge (ESD) occurs when there is a contact with a human body or machine [1-3]. The components or metal wires of a semiconductor integrated circuit (IC) are damaged or destroyed when an ESD surge is applied through an external pin, causing circuit malfunctions. With the rapid development of the high-integration technology of semiconductor devices, the gate-oxide film thickness has gradually decreased owing to the demand for small pin capacitance [4-6]. However, this makes the static electric resistance of the IC very weak. A silicon-controlled rectifier (SCR) is typically used to protect internal ICs from such ESD surges. In general, an SCR-based ESD protection circuit consists of a junction area of an N-well and a P-well. It also has a small parasitic static capacitance and a high current driving capability relative to its area, owing to the operation of two parasitic NPN/PNP bipolar junction transistors (BJTs). However, the SCR has a very high trigger voltage of approximately 20 V because it has an avalanche breakdown between wells, owing to its structural characteristics; moreover, it has a low holding voltage of approximately 1.5 V because of its relatively high current gain [7, 8]. Therefore, the trigger voltage of SCR needs to be improved to prevent the destruction of the gate-oxide film in the internal circuit, and the latch-up immunity characteristics must be secured by improving the low holding voltage characteristics. However, the traditional method of length increment can increase the discharge length of the ESD current, leading

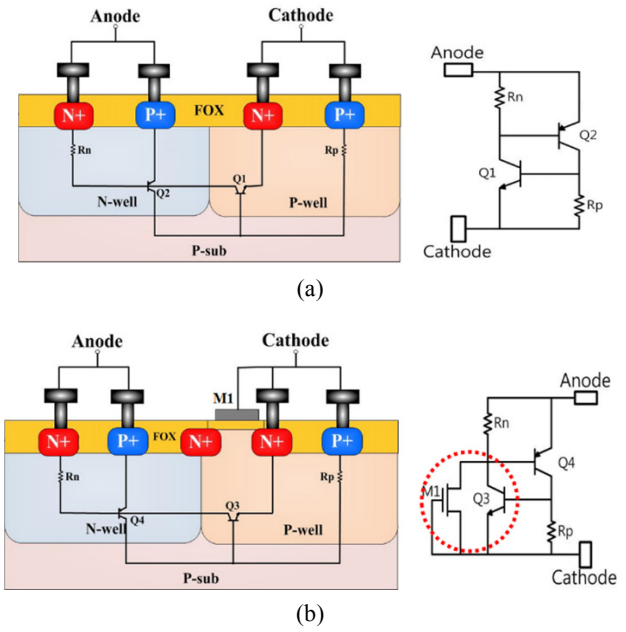



**Fig. 1.** Cross-sectional view and equivalent circuit of (a) typical SCR, (b) LVTSCR.

to a reduced dynamic resistance of the ESD protection circuit. Therefore, this paper proposes an SCR-based ESD protection circuit with high robustness, a high holding voltage, and a low trigger voltage resulting from an additional parasitic NPN BJT operation.

## II. Proposed ESD Protection Circuit

A typical SCR consists of a PNPN structure, as shown in Fig. 1(a). Fig. 1(b) shows a low-voltage-triggered SCR (LVTSCR) reported in a previous study to improve the trigger and holding voltages of a typical SCR [9, 10]. The LVTSCR decreases the high trigger voltage of the SCR. Numerous studies on this structure have been conducted. The LVTSCR induces a low trigger voltage by forming an NMOSFET at the cathode end (red dotted circle), leading to the generation of an avalanche breakdown point at high concentration. Similar to a typical SCR, the LVTSCR operates in the latch mode of two parasitic bipolar transistors (Q3, Q4). Its electrical characteristics are improved by minimizing the effective base of an NPN parasitic bipolar transistor (Q4) to the gate region of the inserted NMOSFET. However, the LVTSCR has a slightly reduced holding voltage than the typical SCR because of its small base, which may cause a latch-up issue.

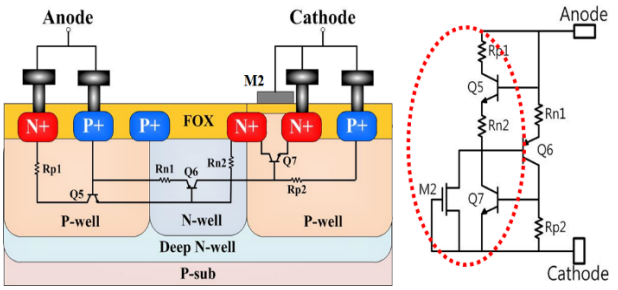



**Fig. 2**. Cross-sectional view and equivalent circuit of the proposed SCR, which has an additional NPN parasitic bipolar transistor.

### 2. Structure and Operational Principle of the Proposed SCR-based ESD Protection Circuit

Fig. 2 shows the cross-sectional view and equivalent circuit of the proposed SCR-based ESD protection circuit. The proposed SCR-based ESD protection circuit is formed on a deep N-well to block a P-type leakage path. A P+ implant is formed on the left side of the center of the N-well area and an N+ implant is formed on the right side of the center of the N-well area. The P+ implant region on the left supports the forward junction, and the N+ implant region on the right increases the doping concentration at the avalanche breakdown point to lower the trigger voltage of the device. In addition, an NMOSFET structure is formed at the cathode region as in the LVTSCR to minimize the base region of the parasitic NPN bipolar transistor (Q3), leading to a minimized gate length.

The operation principle of the proposed SCR-based ESD protection circuit is as follows. In the normal operation region of an internal IC, the proposed SCR does not operate because of the high potential of the forward junction in the N+ bridge region at the right side of the center and the P-well region on the right side. On the other hand, when an ESD surge is applied, the electron current increases the potential of the N-well and an avalanche breakdown occurs when a threshold is reached. The electron-hole pair created by the reverse junction triggers the PNP parasitic BJT (Q6), and the current of a parasitic PNP BJT (Q6) increases the potential of the P-well structures on the left and right sides. Thus, the potential of the N-well increased by the parasitic PNP BJT (Q6) base-emitter junction is forward-biased, and two parasitic NPN BJTs (Q5, Q7) are turned on. Therefore, the latching operation of three parasitic

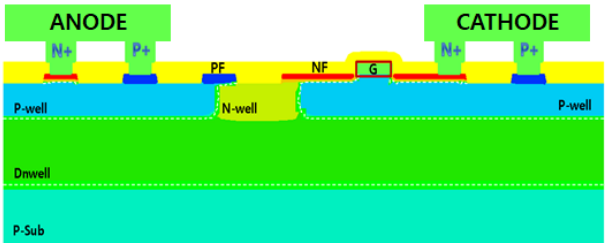



**Fig. 3.** Structure of the proposed SCR, which is implemented through 2D TCAD simulation.

BJTs (NPN (Q5, Q7) and PNP (Q6)) can be triggered by positive feedback, and the ESD current can be effectively discharged at a voltage higher than the ESD current. In particular, an additional NPN parasitic bipolar transistor (Q5) exists on an ESD discharge path and increases the voltage drop across the proposed SCR to induce a significant increase in the holding voltage. Therefore, compared to the existing SCR devices, the path of the NPN parasitic bipolar transistor is formed toward the surface, and the NPN bipolar transistor with a relatively higher current gain can minimize the increase in dynamic resistance and robustness deterioration due to the increased current discharge length.

A two-dimensional (2D) TCAD simulation was performed to demonstrate the operation mechanism of the proposed SCR. Fig. 3 shows the structure of the proposed SCR implemented through simulation [11, 12]. A human body model (HBM) 4 kV ESD surge formed at 100 pF and 1.5 kΩ was applied to the proposed device, as shown in Fig. 4(a) to verify the operation principle of a device under ESD stress. In addition, Fig. 4(b)-(e) shows the overall current flow before triggering, at the triggering point, after triggering, and under the fully turned-on state. Before triggering, a leakage current is observed, owing to the potential of the reverse junction. After triggering, a current flows through the N+ region on the left, and a current path between the PNP parasitic bipolar transistor (Q6) and two parasitic NPN BJTs (Q5 and Q7) is formed. At this time, the current path of the two NPN BJTs is formed close to the surface at the bottom of the gate, and an SCR path is formed deep into the substrate in the fully turned-on state.

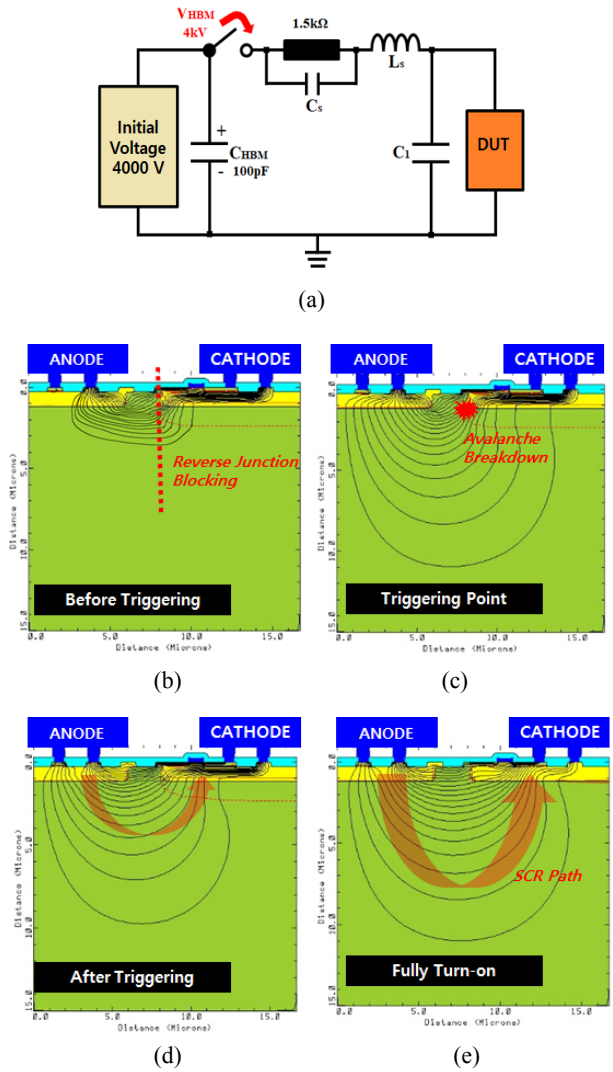



**Fig. 4.** (a) Equivalent circuit of mixed simulation to provide HBM pulse and overall current flow per operation point of the proposed SCR, and current flow images, (b) before triggering, (c) at the triggering point, (d) after triggering, (e) under the fully turned-on state.

## III. Measurement Results

### 1. Device Fabrication and TLP Measurement

The proposed SCR-based ESD protection circuit, SCR, and LVTSCR are fabricated using a 0.18 μm bipolar-CMOS-DMOS (BCD) process, and they have the same width for a fair comparison of their electrical characteristics. Fig. 5 shows the layouts of the fabricated devices and a 50× magnified image of the proposed device. In addition, transmission line pulse (TLP) measurements were used to verify the electrical characteristics and robustness [13, 14]. Fig. 6 shows the

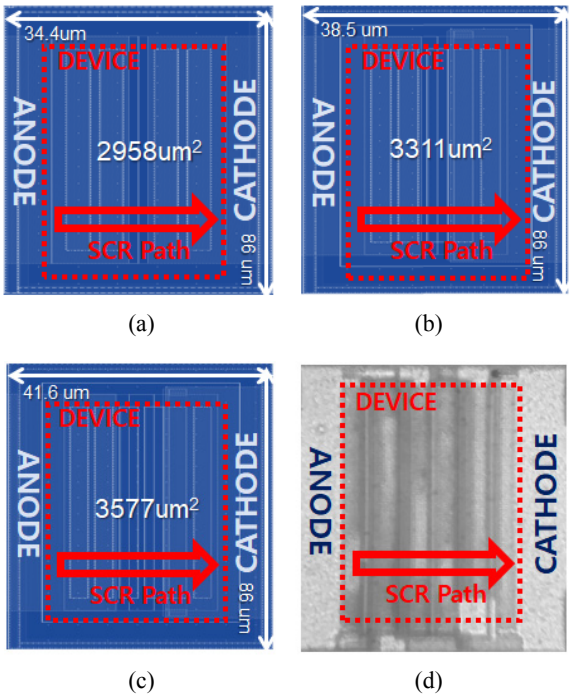



**Fig. 5.** Layout of the existing devices per 0.18 µm BCD process (a) SCR, (b) LVTSCR layout, (c) layout of the proposed device, (d) 50× magnified image.

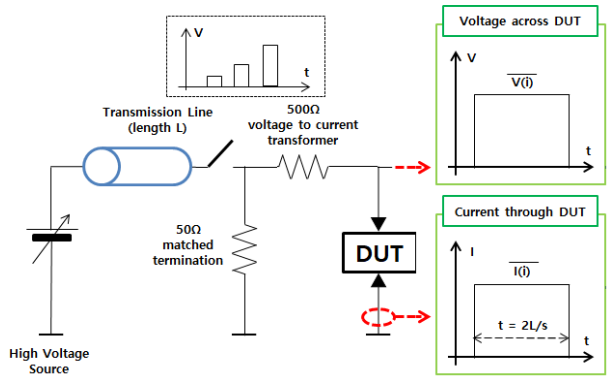



**Fig. 6.** Operational principle of the TLP system.

measurement environment of the TLP system. The square pulse charged with an internal parasitic capacitance rises gradually and is applied to the device under test (DUT). The current flowing through the DUT and the DUT voltage are measured using the current and voltage probes, respectively. TLP systems are widely used to measure the electrical properties and robustness of ESD protection devices, with a pulse width of 100 ns and a rise time of 10 ns in this experiment.

Fig. 7 shows the TLP *I-V* measurement results of SCR, LVTSCR, and the proposed ESD protection device. In the 0.18 µm BCD process, an ESD design window for 5-V

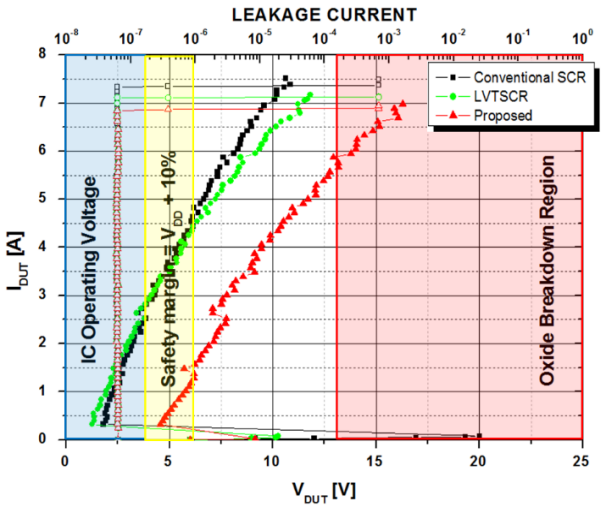



**Fig. 7.** Waveforms from the TLP measurement of DUTs.

**Table 1.** Summary of the DUT snapback characteristics

| Structure | Electrical Characteristics | | | |
|---|---|---|---|---|
| | $V_T$ [V] | $V_H$ [V] | $I_{t2}$ [A] | Direction |
| SCR | 20.1 | 2.07 | 7.49 | One |
| LVTSCR | 10.3 | 1.31 | 7.12 | One |
| Proposed | 9.14 | 4.55 | 6.98 | One |

application is formed between an operating voltage margin of +10% and the gate-oxide breakdown region of 12.5 V. From the TLP measurement results, the proposed ESD protection circuit was observed to have a trigger voltage of 9.14 V, which is lower by 20.1 V compared with that of SCR and 10.3 V compared with that of LVTSCR. The circuit has a high holding voltage of 4.55 V. In addition, it still has an exceedingly high secondary trigger current ($I_{t2}$) of approximately 7 A, owing to the operation of two parasitic NPN bipolar transistors that have a relatively high current gain. Table 1 summarizes the electrical characteristics of the fabricated ESD protection devices.

## 2. Optimization of Electrical Characteristics of the Proposed SCR-based ESD Protection Circuit

Although the holding voltage of the proposed ESD protection circuit is relatively high, it can be optimized for 5-V class applications by using the design parameters D1 and D2 shown in Fig. 8. D1 represents the distance between two bridge regions and can be used to adjust the effective base region of a PNP parasitic bipolar transistor (Q6). This can induce an increase in the holding voltage.

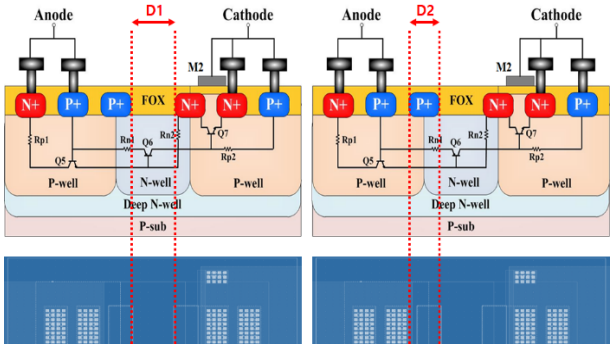



**Fig. 8**. Design parameters of the proposed ESD protection circuit (a) D1, (b) D2.

However, an increase in D1, which has a relatively low doping concentration, causes an increase in the resistance of the ESD discharge path, which causes a significant decrease in the robustness in the ESD mode. On the other hand, the design parameter D2 is the length of the P+ bridge region of the proposed device, and it can effectively increase the effective base lengths of the additional NPN parasitic bipolar transistor (Q6) and the PNP parasitic bipolar transistor (Q5) of the proposed device simultaneously. Fig. 9 shows the TLP waveforms with the D1 and D2 of LVTSCR increased by 3 μm each. As the length of the design parameter D1 increased from 5 μm to 14 μm, the holding voltage increased from 4.55 V to 6.29 V. As the length of the design parameter D2 increased from 4 μm to 13 μm, the holding voltage significantly increased up to 6.60 V. In addition, the on-state resistance showed a relatively smaller increase for the same increase in the length of D2 due to the influence of the NPN parasitic bipolar transistor path, which has a higher current gain compared to D1. Table 2 summarizes the electrical characteristics of the proposed device depending on the design parameters.

## 3. Experimental Results of Temperature Reliability

The thermal reliability of the proposed ESD protection circuit at high temperatures (300-500 K) is shown in Fig. 10. In the thermal reliability test, the water is heated by a hot-chuck control system, and the TLP system evaluates its electrical characteristics [15, 16]. The high-temperature characteristics affect the electrical characteristics and $I_{t2}$ of an ESD protection device. As

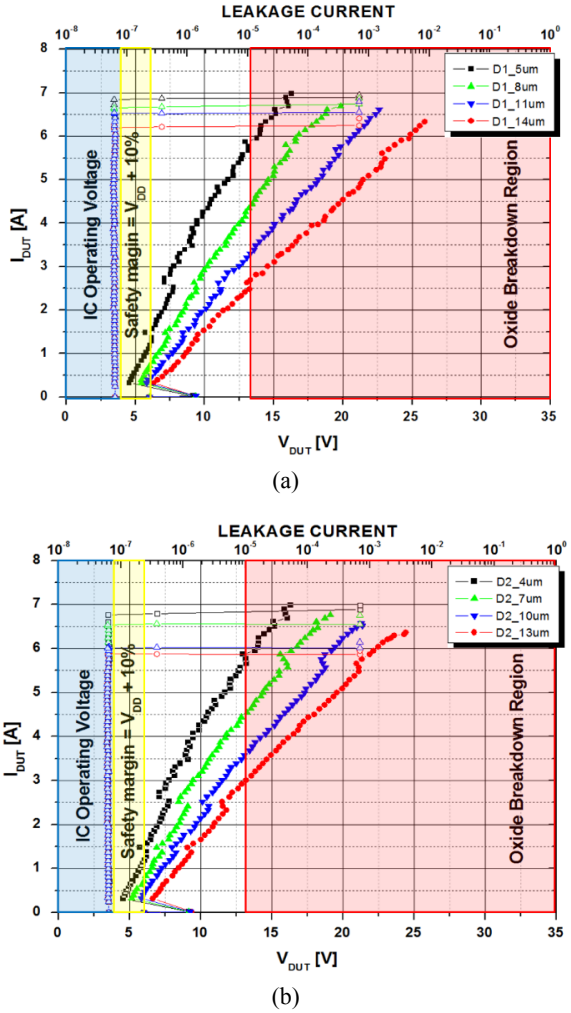
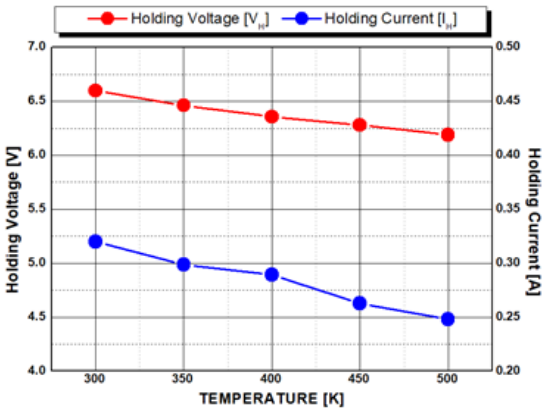



**Fig. 9.** TPL waveforms according to the increase in the design parameters (a) D1, (b) D2.

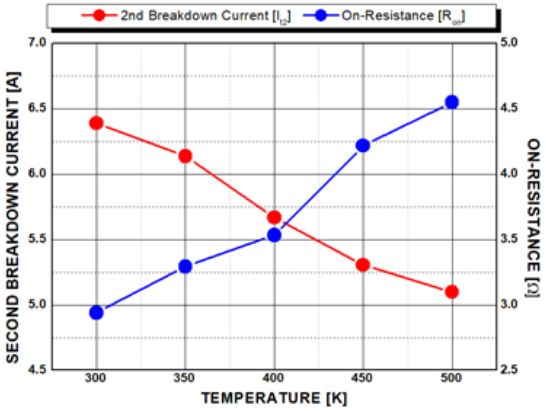
**Table 2.** Summary of the electrical characteristics of the proposed device per design parameters (D1, D2)

| Structure | Design Parameter [μm] | | Electrical Characteristics | | |
|---|---|---|---|---|---|
| | | | $V_T$ [V] | $V_H$ [V] | $I_{t2}$ [A] |
| Proposed ESD Clamp | D1 | 5 | 9.14 | 4.55 | 6.98 |
| | | 8 | 9.16 | 5.42 | 6.86 |
| | | 11 | 9.21 | 5.80 | 6.78 |
| | | 14 | 9.27 | 6.29 | 6.40 |
| | D2 | 4 | 9.14 | 4.55 | 6.98 |
| | | 7 | 9.14 | 5.13 | 6.79 |
| | | 10 | 9.24 | 5.82 | 6.52 |
| | | 13 | 9.33 | 6.60 | 6.39 |

the temperature increases, the carrier mobility decreases, the resistance of the well region increases, and consequently, the heat losses of both the on-resistance of the ESD protection device and $I_{t2}$ occur. In addition, after




(a)




(b)

**Fig. 10.** Measured results of high-temperature (300-500 K) reliability of the proposed device (a) holding voltage and current, (b) secondary trigger current and on-resistance.

the avalanche breakdown, the holding current decreases because of the increase in the resistance component at both ends of the device, and the base emitter voltage of the parasitic NPN/PNP BJT decreases, thereby reducing the holding voltage. This experiment evaluated a structure with a D2 of 13 µm whose holding voltage was optimized to be suitable for a 5-V class ESD design window. From the measurement results, the proposed device was observed to maintain a high holding voltage of 6.2 V at a temperature of 500 K, which is higher than 5.5 V, the safety margin of the operating voltage of an internal IC + 10%. The proposed device also had a secondary trigger current of 5.1 A and a high robustness of over HBM 6 kV (calculated as $(1500+R_{on})*I_{t2}$). Therefore, the proposed ESD protection device has outstanding thermal reliability and high-temperature characteristics.

## V. CONCLUSIONS

This paper proposed a new SCR structure with improved electrical characteristics of low trigger voltage and high holding voltage. The proposed ESD protection device induces an increased holding voltage by increasing the voltage drop across both ends of a protection circuit by additionally turning on an NPN parasitic bipolar transistor (Q5), which has a higher current gain compared to the existing SCR and LVTSCR, on an ESD discharge path. In addition, Q5 creates a path that is closer to the surface area compared with the NPN parasitic bipolar transistors (Q1, Q3), which are formed inside an existing SCR-based ESD protection circuit; thus, its trigger voltage characteristics can be improved. From the measurement results, the proposed ESD protection device has improved electrical characteristics with a low trigger voltage of 9.14 V and a holding voltage of 4.55 V. It can be optimized to be appropriate for a 5-V class ESD design window by adjusting the design parameter D2, which can simultaneously increase the base areas of two parasitic bipolar transistors (Q5, Q6). In addition, the proposed ESD protection circuit maintained outstanding electrical characteristics at a high temperature of 500 K through a temperature reliability test using a hot-chuck control system. The proposed ESD protection device was fabricated using a 0.18 µm BCD process. It is expected that the proposed device can contribute to cost reduction and reliability improvement through an improvement in area efficiency when applied to 5-V class applications.

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