JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.21, NO.2, APRIL, 2021 ISSN(Print) 1598-1657
https://doi.org/10.5573/JSTS.2021.21.2.109 ISSN(Online) 2233-4866

Handy Calibration Substrate for both Horizontal and Vertical Probing

Bo Pu[1], Taeho Kim[2], Jinho Joo[3], and Wansoo Nah[4]

Abstract—**This article proposes a novel substrate for a handy SG-GS/SG-SG calibration in both horizontal and vertical probing measurement. The proposed substrate provides two ways of probing for "through" calibration in horizontal and vertical positions without changing the probe holders. It has "through" lines vertically and horizontally using vias and traces, respectively, and both "through" lines were designed to satisfy 50 ohms of characterization impedance. A prototype of the proposed substrate was fabricated using FR4 and then tested in the horizontal calibration resulting in the successful reproduction of all the *S*-parameters in the horizontal meander test board. It was also tested in the vertical calibration, and was successful to re-produce all the coupling effects in via arrays, demonstrating the effectiveness and handiness of the proposed calibration substrate.**

Index Terms—**Calibration, vertical through interconnect, calibration kit, impedance standard substrate, microwave probes, short-open-load-through**

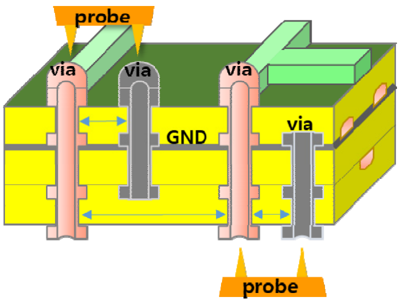
Manuscript received Sep. 9, 2020; reviewed Jan. 5, 2021; accepted Mar. 16, 2021
[1]EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, 65409, USA
[2]LG Innotek, 30, Magokjungang 10-ro, Gangseo-gu, Seoul, 07796, Korea
[3]School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon 16419, Korea
[4]Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea
E-mail : wsnah@skku.edu

I. INTRODUCTION

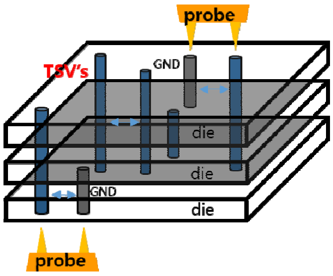
With the trend of miniaturization technology for the electronic equipment, vertical connectors such as pogo pins in probe card for wafer test and vias in multi-layer printed circuit board (PCB) have been widely used in various devices [1]. Moreover, semiconductor technology has been developing dramatically due to successful die stacking technologies in integrated circuits (ICs) using through silicon vias (TSV) [1]. Therefore, vertical connection such as vias in printed circuit board (PCB) or through TSV in 2.5D silicon interposer or 3D chips is necessary for the signal propagation in diverse hierarchical levels, and the signal transfer characteristics from top/bottom to bottom/top plates need to be measured as shown in Fig. 1 [2-5].

Vector Network Analyzer (VNA) has been exclusively used to effectively measure scattering parameters (*S*-parameters) for the characterization of components in electronic devices especially in high frequency range [6]. To ensure the accuracy of measurement by VNA, a calibration is required before error-corrected tests are performed. The common calibration algorithm used for multi-port measurement is known as short-open-load-through (SOLT) or Through-Reflect-Line (TRL) methods [7, 8]. No matter which method we choose, an appropriate through design is crucial to the performance of calibration as the most transmission parameter for error model has been known to be generated in through.

A conventional horizontal thru impedance standard substrate is illustrated in Fig. 2 [9]. The metal surface of kit(substrate) is co-planar type for horizontal probing SG-GS in (a) and SG-SG in (b). Fig. 3 shows two pictures for probing traces/pads on PCB (a) horizontally,

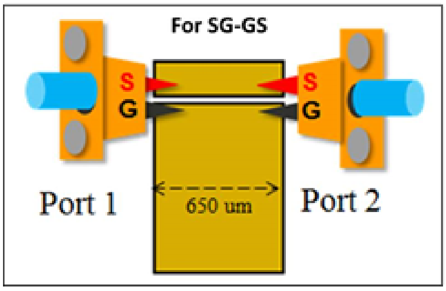


(a)

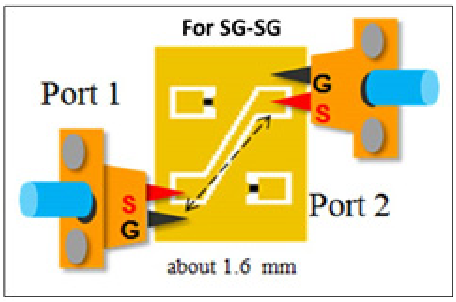


(b)

Fig. 1. (a) Vertical connection in PCB, (b) Vertical connection in 3D integrated circuit, not to scale.



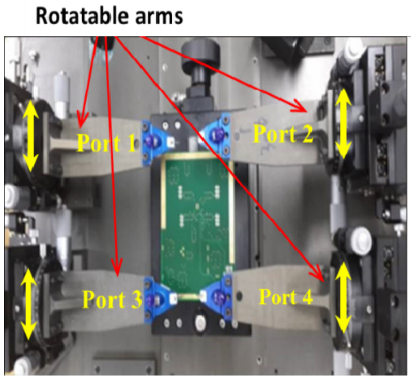
(a)



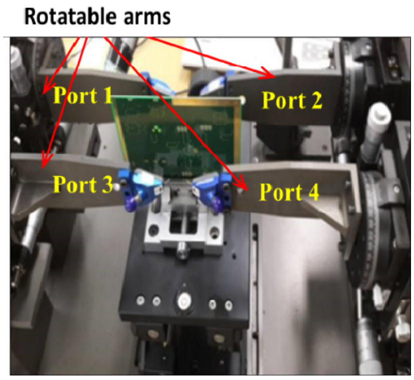
(b)

Fig. 2. Conventional standard kit (substrate) for horizontal thru's (a) SG-GS, (b) SG-SG.

and (b) vertically using specially designed probe station. Note that each arm was designed to slide as indicated by the yellow arrows in Fig. 3(a) to localize the probing point and to be rotated as in Fig. 3(b). For the horizontal



(a)



(b)

Fig. 3. Pictures for probing traces/pads on PCB (a) horizontally, (b) vertically.

calibration in Fig. 3(a), conventional calibration kits in Fig. 2 can be used for thru calibration of Port1-Port2, Port1-Port4, Port3-Port2, and Port3-Port4, but for the calibration of Port1-Port3 and Port2-Port4, we need a vertical thru as described in Fig. 3(b). Without vertical thru, we need to change the probe holder for horizontal calibration and then re-place it back to the original holder. It not only takes time in the calibration process, but also generates a risk of precision degradation caused by changing the position of the probe tips, which is usually very sensitive to the surroundings. So, a novel calibration kit which can be used in both horizontal and vertical connections, is required.

In this paper, we propose a handy calibration substrate for both use of horizontal and vertical probing. The validated frequency of the specific proposed calibration substrate is around 8 GHz using FR4 as a substrate, and it is very handy to use especially for the calibration of both vertical and horizontal probing. Section II introduces the theoretical background of thru and proposes novel thru structure with its experimental data.

Implementation of the proposed kit on the horizontal and vertical interconnects is discussed in Section III. Ultimately, a conclusion is described in Section IV.

II. Theoretical Background and Proposed Structure

The characteristic impedance of a transmission line can be described as (1) using two port S-parameters.

$$Z_C(\omega) = Z_0 \sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} \tag{1}$$

, where Z_C and Z_0 are the characteristic impedance of the transmission line and reference impedance of the system, respectively. Propagation constant of a transmission line is able to be derived by the *S*-parameters and length of transmission network as in (2),

$$\gamma = \alpha + j\beta = \frac{1}{l}\cosh^{-1}\left(\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}^2}\right) \tag{2}$$

, where γ: propagation constant (1/m), α: attenuation constant (Neper/m), β: phase constant (rad/m), and l: length of transmission line (m).

An ideal thru in impedance standard substrate is a transmission line with zero-length, no reflection and performs pure transmission of signals. However, a through in the realistic scenario has a finite length, and reflection could be caused by impedance mismatch, and loss in transmission. The thru calibration standard is used for obtaining the transfer characteristics between two ports. Electrical length of a thru affects the phase of propagated signal, and generates a bias in the phase. The phase bias is able to be compensated in the calibration by propagation constant in thru, which cancels the phase bias exactly. Compensated propagation constant is derived from the measured *S*-parameters of the thru line on the basis of (2).

The proposed through substrate has two sides (surfaces), with the same pattern in each. Each surface has a symmetrical structure, and three vias, two for grounds and one for signal, were used to connect both sides as illustrated in Fig. 4. Fabricated calibration kit with SOLT impedance standard substrates is shown in

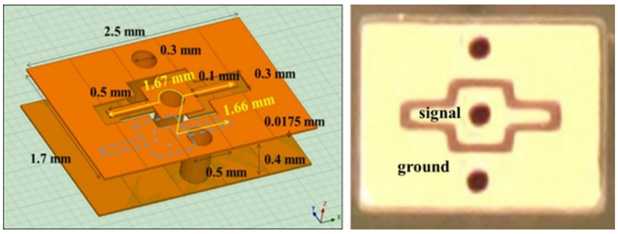


Fig. 4. Proposed through structure for calibrations in both horizontal and vertical interconnectors.

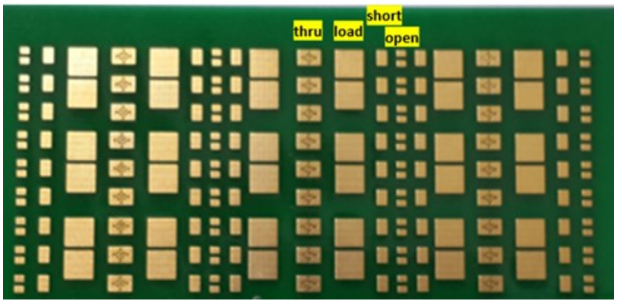


Fig. 5. Fabricated calibration kit with proposed thru, short, open, and load impedance standard.

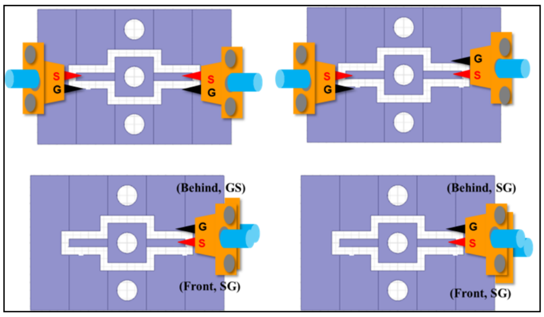


Fig. 6. Calibration for diverse probing types (horizontal probing on the same plane for the upper two cases, and vertical probing on different planes for the lower two cases).

Fig. 5, where the thru, load, short, and open are located. For the easiness in fabrication, the substrate was designed with FR-4 material and copper for the dielectric and trace conductors, respectively. Length of pad edge and via thickness were intentionally designed as 0.5 mm and 0.4 mm, respectively, to provide the similar distance for signal propagation in horizontal and vertical traces. Note that thru has the same vertical and horizontal length of 1.66 (1.67) mm as in Fig. 4.

Fig. 6 illustrates locations of probes for SG-GS thru calibration on the same plane (upper/left), SG-GS on the front and behind planes (lower/left), SG-SG on the same plane (upper/right), and SG-SG on the front and behind planes (lower/right), demonstrating the versatility of the

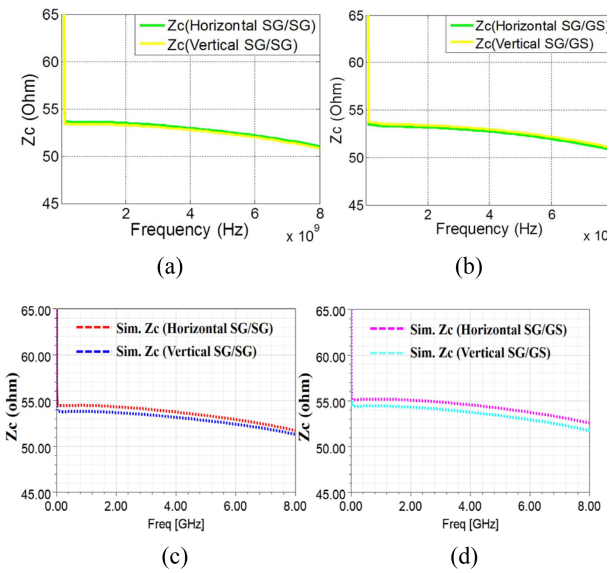


Fig. 7. Characteristic impedance of the thru's up to 8 GHz (a) and (b) are from measured *S*-parameters, (c) and (d) are from full wave simulated *S*-parameters.

proposed thru substrate. Characteristic impedance (Z_C) of the thru's which were obtained from (1) using *S*-parameters are shown in Fig. 7(a)-(d): the *S*-parameters of (a) and (b) are from measurement, and those of (c) and (d) are from full wave EM-simulation. In the measurement, one can find that Z_C in the horizontal thru does coincide with Z_C in the vertical thru for both SG-GS and SG-SG calibration as well. Single-ended Z_C of the proposed thru is 51~53 Ω in the frequency range from 300 kHz to 8 GHz for SG-SG and SG-GS in both horizontal and vertical thru's. Tolerance of the manufacturing process is 200 μm for via diameter, and 100 μm for pad size. In the full wave EM simulation, less than ~1 Ω discrepancy (0.6 Ω ~ 0.8 Ω @ center of bandwidth 4 GHz) was observed for the horizontal and vertical thru's which seems to be negligible.

Comparison of reflection and insertion loss characteristics of the proposed and conventional commercial Cascade calibration kit is illustrated in Fig. 8. In this case, VNA was calibrated using SG-GS commercial calibration kit shown in Fig. 2, and then S_{11} and S_{21} have been measured for the Cascade and for the proposed SG-GS thru's as well. Because VNA has been calibrated using Cascade thru, S_{11} of SG-GS Cascade thru is very tiny, ideally zero, and the large phase fluctuation in Fig. 8(a) is due to the small size of S_{11}. The return loss of the proposed thru is higher than that of

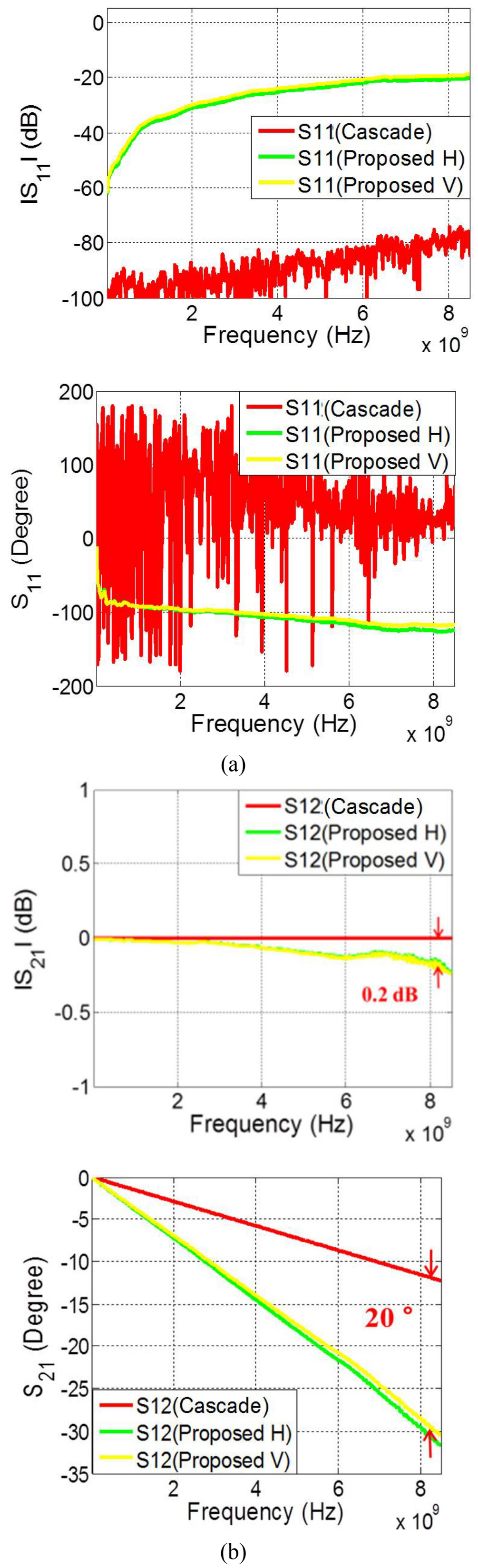


Fig. 8. Comparison of (a) reflection characteristics, (b) insertion loss characteristics of commercial and proposed SG-GS thru's.

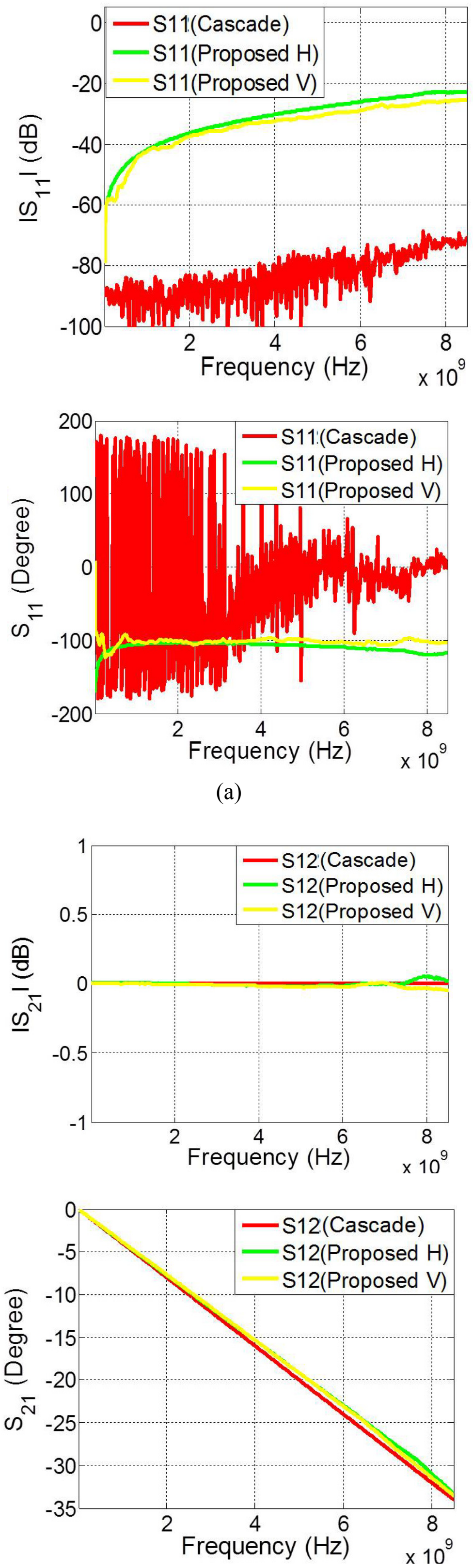


Fig. 9. Comparison of (a) reflection characteristics, (b) insertion loss characteristics of commercial and proposed SG-SG thru's.

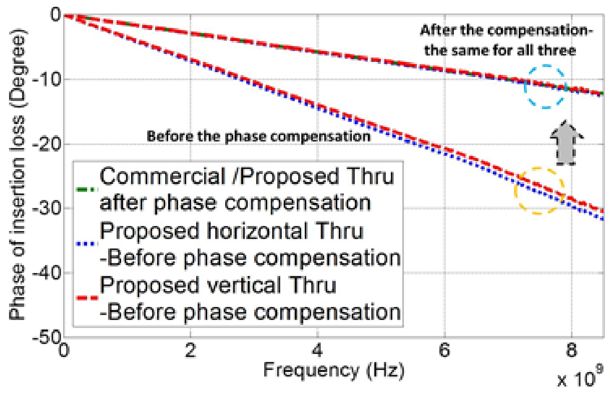


Fig. 10. Insertion loss-S21 magnitude and phase of SG-GS thru substrates: phase bias has been compensated.

commercial kit, but it is still acceptable (less than -20 dB). Fig. 8(b) illustrates the comparison of insertion loss between the proposed and Cascade thru's. The insertion loss of SG-GS Cascade thru stays 0 dB in the whole frequency range: this is again due to the fact that VNA was calibrated using Cascade thru. The maximum difference in VNA insertion loss is ~0.2 dB in magnitude and ~20° in phase from 300 kHz up to 8 GHz. The large phase difference in S_{21} is due to the difference in length: 650 μm for SG-GS thru in Cascade while 1,670 μm for SG-GS in the proposed one.

Length of thru's are intentionally designed to be around 1,670 μm for both SG-GS and SG-SG in our proposed substrate, and it could be a merit which maintains the same propagation bias in different probing scenarios while commercial one cannot in this specific case (650 μm for SG-GS and 1,650 μm for SG-SG).

In SG-SG probing, return loss shows similar results to those in SG-GS probing as described in Fig. 9(a), and no difference of magnitude and phase of insertion loss are observed as shown in Fig. 9(b): this is because the lengths of thru's are same in both commercial and the proposed thru's.

As in Fig. 8(b), there is a phase difference due to the length difference between the commercial and proposed SG-GS thru substrates. The phase bias is able to be compensated if we know the propagation delay in length. The compensated insertion loss in commercial SG-GS probes is illustrated in Fig. 10: after the compensation in length, the phase of the insertion loss moves up to the point of the commercial thru. It is good to see that the two data from horizontal and vertical thru's coincide very well in all cases, which means they are equivalent

Table 1. Group delay for commercial and proposed thru cases in SG-GS and SG-SG scenarios.

	Group Delay (ps)	
Probing Type	SG-GS	SG-SG
Commercial thru	6	11.1
Proposed thru	11.1	11.1

even though the geometrical shapes are different from each other.

Generally, a VNA has an option for the compensation of phase difference. The option can be expressed as a group delay, which can be calculated as in (3).

$$t_{group} = \frac{d\beta}{d\omega} \cdot l \tag{3}$$

, where t_{group}: group delay (s), β: phase constant (rad/m), and l: length of transmission line (m).

The derivative in (3) can be calculated from (2). Table 1 summarizes the average group delays including the group delay of commercial SG-GS substrate. One can find that the group delays in both SG-GS and SG-SG are same in the proposed substrate, but are different in commercial substrates.

III. Implementation and Validation of Proposed Thru Impedance Standard Substrate

In order to validate the proposed thru substrate, firstly we performed *S*-parameter measurement on the basis of designed symmetrical meander lines. Symmetrical meander lines have the characteristic of dense structure with high coplanar inductive coupling and is suitable for the signal-ground probing. The design and abrication of meander lines were discussed in [11], and DUT here has a width of 1.25 mm, a length of 5 mm, and 17 turns. The PCB is one-sided and is composed of FR-4 and copper. S-parameters of meander line were measured after calibration using commercial standard kit and the same S-parameters were measured after calibration using proposed impedance substrates, and then the two S-parameters were compared. The characteristics of measured meander lines on the basis of SG-GS probing are illustrated in Fig. 11. Measured S-parameters using the commercial calibration kit and the proposed one

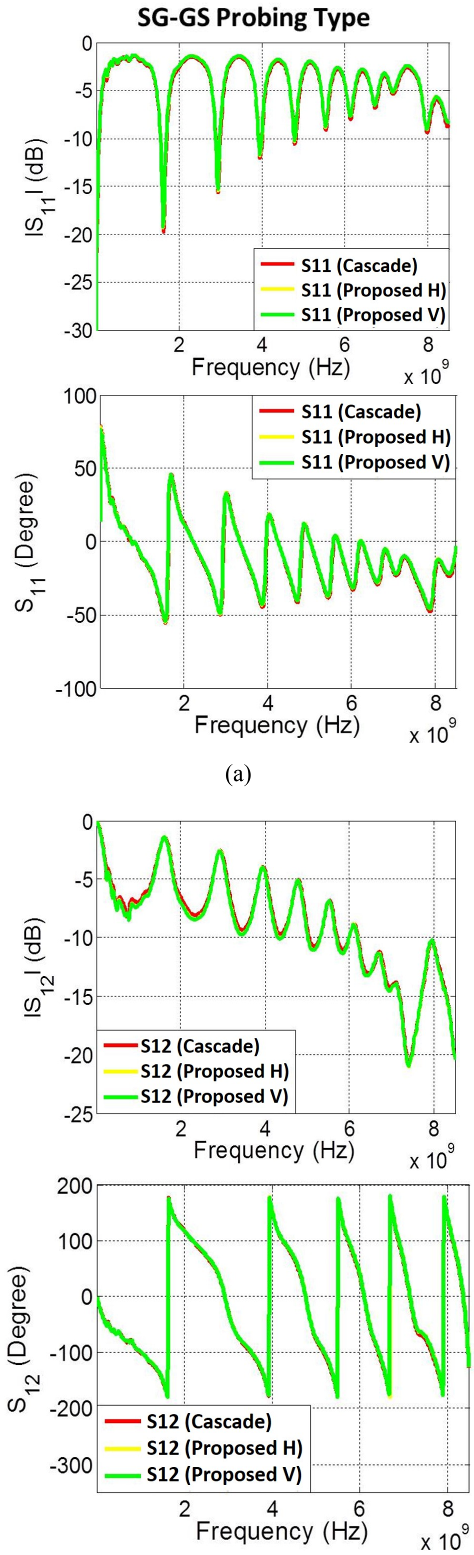


Fig. 11. Measured S-parameters of meander lines using commercial and proposed calibration kits. SG-GS thru substrate was used. (a) return loss, (b) insertion loss of meander lines.

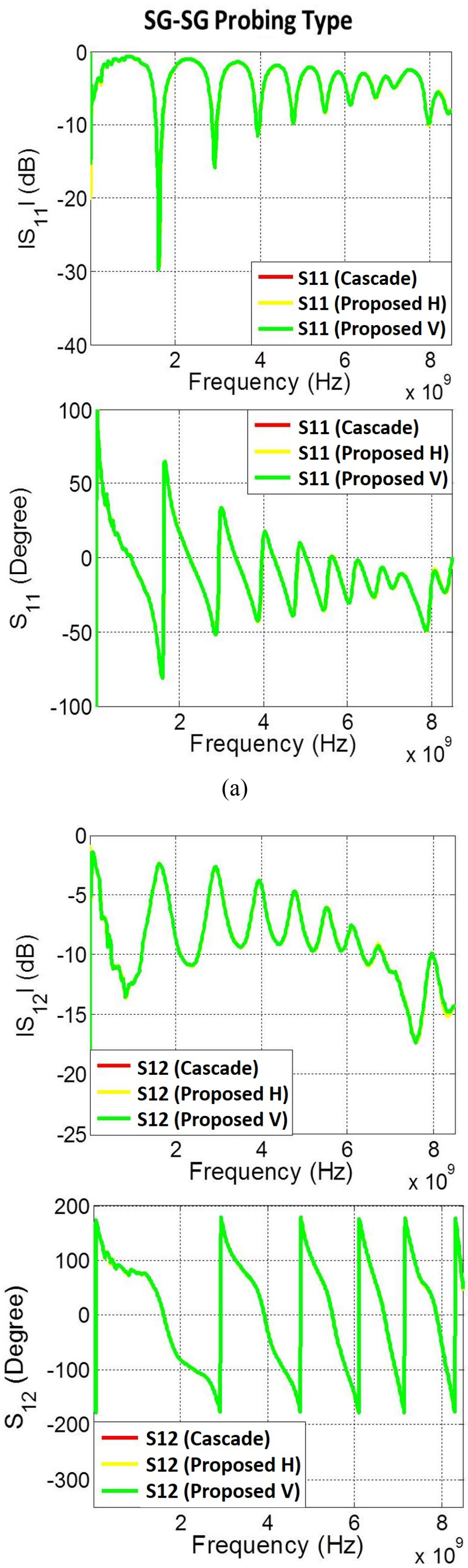


Fig. 12. Measured *S*-parameters of meander lines using commercial and proposed calibration kits. SG-SG thru substrate was used. (a) return loss, (b) insertion loss of meander lines.

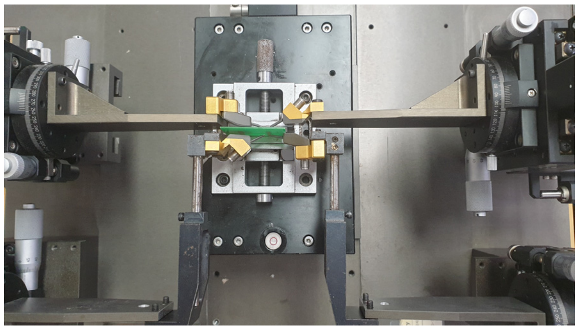
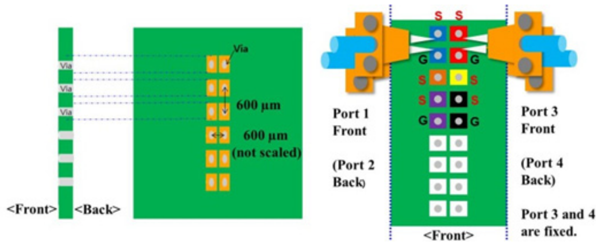


Fig. 13. Setup for measurement of coupling effect in via arrays on PCB.



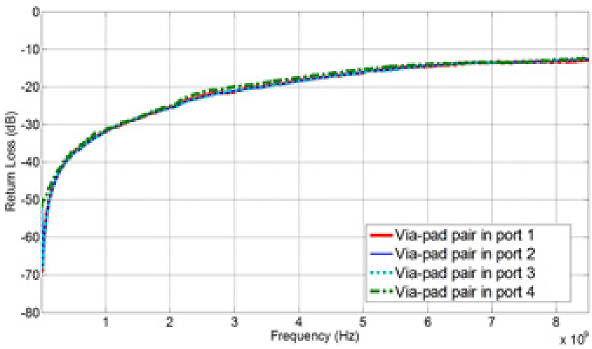
(a) (b)

Fig. 14. Via-pads in PCB for the measurement of coupling effects in the vias (a) top view on the PCB with cross-sectional view, (b) four probes to measure coupling effects between port1-port2 and port3-port4.

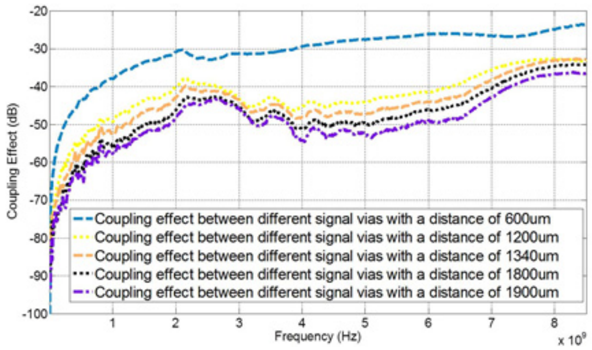
turned out to match each other almost perfectly up to 8 GHz for both magnitude and phase. The same good agreement for the SG-SG probing is also found in Fig. 12. It has been validated that the proposed calibration substrate can achieve the same performance up to 8 GHz as the commercial ones do, still keeping the merit for both use of horizontal and vertical calibration. As a result, the proposed kit is appropriate for handy and accurate calibration up to 8 GHz.

Not only the coplanar coupling but also the vertical coupling generated in the vias of PCB or TSV in silicon substrate are also widely used [12]. As mentioned previously, the conventional coplanar calibration kit is only able to provide a calibration in the same plane. Rotation of probes and location change of cables is inevitable, and the proposed substrate can be conveniently used without changing location of the probes being used, which is very handy and enhances the accuracy of measurement.

The second case study is about the coupling effects of the vertical pins. Arrayed vias in the PCB is shown in Fig. 14 to measure the couplings between the vias, and measurement setup is shown in Fig. 13 as well. The vias



(a)



(b)

Fig. 15. (a) S_{11} of via-pad pair in port 1, 2, 3 and 4, (b) S_{21} between signal vias with distances of 600 μm, 1200 μm, 1340 μm, 1800 μm and 1900 μm, respectively.

are located on the PCB with an interval of 600 μm (diameter: 0.2 mm). The port 3 and port 4 are fixed at the red pads in Fig. 14(b), and the port 1 and port 2 moves to increase the distance between the signal vias: blue (from red to blue: 600 μm) → yellow (from red to yellow: 1200 μm) → orange (from red to orange: 1340 μm) → black (from red to black: 1800 μm) → purple (from red to purple: 1900 μm)). Thus, the characteristics of each via pair (signal-ground) and the coupling effects between different via-pad pairs are able to be measured. Fig. 15 describes the coupling effects of the arrayed vias after calibration using the proposed thru. The data clearly shows that the further the vias, the less the coupling becomes in all the frequency range, which is reasonable in the qualitative point of view. Since it was confirmed that the three calibration thru's (one is the commercial thru, and the other two are proposed horizontal and vertical thru's) are equivalent with one another in the first case study (Fig. 14 and 15), it can be concluded that the data in Fig. 15(b) is the right coupling data in the arrayed vias on PCB.

IV. CONCLUSIONS

In this paper, a handy novel impedance substrate, for the calibration on both horizontal and vertical interconnects are proposed. Unlike the conventional commercial calibration kit which allows probing on the planar plane only, the proposed kit has a vertical structure that makes probing on the opposite sides possible. Therefore, rotation of probe and location change of cables are not necessary. Theoretical analysis and design of the SOLT impedance substrate, especially for the thru case were demonstrated.

The performance of the proposed substrate was validated by the measured return and insertion losses after calibration using conventional and proposed substrate, respectively. The proposed substrate shows high accuracy up to 8 GHz in this specific fabrication using FR4, and it is expected that the frequency limit could be enhanced great with low loss substrate such as alumina and with suitable optimization of the substrate as well. Since the proposed calibration substrate can be used with all the combination of the probes (SG-GS, GS/SG, GS/GS or SG-SG probes) and the location of the ports (horizontal or vertical), our proposed thru could be very useful in the extraction of coupling effect for the vertical connectors such as pogo pins and through silicon vias. Note that the proposed substrate is not for replacing the standards kit, but provides a very handy way to calibrate both horizontal and vertical interconnects keeping reasonable accuracy in the designated frequency range.

ACKNOWLEDGMENTS

This work was supported by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government(MSIT) (No. 2020-0-00960,Development of THz 3-dimensional beamforming systems using distributed feeding of meta antenna for 6G mobile communication.)

REFERENCES

[1] J. H. Lau, Through-Silicon via for 3D Integration, New York, NY, USA:McGraw-Hill, 2013.

[2] S. Pan and J. Fan, "Characterization of via

structures in multilayer printed circuit boards with an equivalent transmission-line model", *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 5, pp. 1077-1086, Oct. 2012.

[3] J. Kim, J. Cho, J. Kim, J.-M. Yook, J. C. Kim, J. Lee, et al., "High-Frequency Scalable Modeling and Analysis of a Differential Signal Through-Silicon Via", *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 4, no. 4, pp. 697-707, April 2014.

[4] E.-P. LI, X. Wei, A. C. Cangellaris, E.-X. Liu, Y. Zhang, M. Damore, et al., "Progress Review of Electromagnetic Compatibility Analysis Technologies for Packages Printed Circuit Boards and Novel Interconnects", *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 248-265, May 2010.

[5] B. Pu, K. Kim and W. Nah, "Package design methodology in consideration with signal integrity, power integrity and electromagnetic immunity," 2014 XXXIth URSI General Assembly and Scientific Symposium (URSI GASS), Beijing, 2014, pp. 1-4.

[6] R. B. Marks, "A multiline method of network analyzer calibration", *IEEE Trans. Microw. Theory Tech.*, vol. 39, no. 7, pp. 1205-1215, Jul. 1991.

[7] U. Stumper, "Uncertainties of VNA S-parameter measurements applying the short–open–load–reciprocal (SOLR) calibration method", *CPEM Conf. Dig.*, pp. 438-439, 2008.

[8] J. Fleury and O. Benard, "Designing and characterizing TRL fixture Calibration standards for device modeling", *Appl. Microw. Wirel.*, vol. 13, no. 10,2001, pp. 26-55.

[9] Mostafa Emam. RF Characterization – The approach and the advantages, MOS-AK Tutorial Day – Shanghai, June 26, 2016.

[10] Pozar, David M. "Microwave engineering, 3rd." Danvers, MA: Wiley (2005).

[11] B. Pu, K. H. Kim, S. Kim and W. Nah, "Modeling and Parameter Extraction of Coplanar Symmetrical Meander Lines", *Electromagnetic Compatibility IEEE Transactions on,* vol. 57, no. 3, pp. 375-383, June 2015.

[12] S. Wu and J. Fan, "Analytical prediction of crosstalk among vias in multilayer printed circuit boards", *IEEE Trans. Electromagn. Compat.*, vol. 54, pp. 413-420, Apr. 2012.

[13] D. Seo, H. Lee, M. Park, and W. Nah, "Enhancement of Differential Signal Integrity by Employing a Novel Face Via Structure," *IEEE Trans. Electromagn. Compat.*,, vol. 60, no. 1, pp. 26-33, Feb. 2018.

Bo Pu received the B.S. degree in electrical engineering from the Harbin Institute of Technology, China, in 2009, and the Master & Ph.D. degree in electronic and electrical engineering from Sungkyunkwan University, South Korea, in 2015. From 2015 to 2020, he worked for Foundry Business, Semiconductor R&D Division of Samsung Electronics, Hwaseong, Korea, as a Staff Engineer. In July 2020, He joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently a visiting assistant research professor of National Science Foundation (NSF) Industry/University Cooperative Research Center for Electromagnetic Compatibility. His research interests include the design methodology for chip-package-PCB systems in areas of signal/power integrity and EMC. He recently focuses on the research of high-speed integrated circuits system up to 224 Gbps, 2.5D Si-interposer for high bandwidth memory (HBM), and through silicon via (TSV) for 3-D ICs. He holds 10 patents about high-speed links and 2.5D/3D ICs. Dr. Pu was the recipient of Best Student Paper Award at the IEEE APEMC 2011 and a Young Scientists Award from the International Union of Radio Science (URSI) in 2014, and the 2019 Distinguish reviewer for IEEE Transactions on Electromagnetic Compatibility. He also obtained Ph.D. Fellowship Award in 2013, Best Innovation Award, Excellent Performance Award, and Excellent Project Award as the first awardee in 2015-2019 from Samsung Electronics. He served as a Session Chair in IEEE APEMC 2017, IEEE EMC+SIPI 2020, and a TPC Member of the Joint IEEE EMCS & APEMC 2018. He is an Associate Editor for IEEE Access and moderator of IEEE TechRxiv as well as a Senior Member of IEEE.

Taeho Kim Taeho Kim received his B.S. degree in electrical engineering from the Kumoh National Institute of Technology, Korea, in 2011, and the Master degree in electronic and electrical engineering from Sungkyunkwan University, South Korea, in 2014. He is currently working for LG Innotek, Seoul, Korea, since 2015 as a senior engineer. His research areas include EMI/EMC, Currently, his research includes SI/PI on Camera Module

Jinho Joo received his Ph.D. degree from the Illinois Institute of Technology, USA in 1993. He is a professor in the School of Advanced Materials Science and Engineering, Sungkyunkwan University, Korea, since 1995. He has authored 157 papers in international and domestic journals. His current research focuses on two areas: the syntheses of nanostructure materials (ZnO, IGZO, TiO_2, and MoS_2) for LED, photocatalyst, and gas sensor applications, and the electromagnetic interference/calibration system analysis.

Wansoo Nah received B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1984, 1986, and 1991, respectively. Since 1995, he has been with Sungkyunkwan University, Suwon, South Korea, where he is currently a Professor with the College of Information and Communication Engineering. He was a Senior Researcher with the Korea Electrical Research Institute, Changwon, South Korea, from 1991 to 1995. His primary research interests include electromagnetic interference/compatibility system analysis and design.