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A 87.5-dB-SNDR Residue-integrated SAR ADC with a Digital-domain Capacitor Mismatch Calibration

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Abstract—**This paper presents an asynchronous-clocking 16-bit successive approximation register (SAR) analog-to-digital converter (ADC) suitable for high-precision sensor applications. Comparator noise and nonlinearity from capacitor mismatch, as two major performance-limiting problems of SAR ADC, are resolved by noise averaging with a residue integration and a digital-domain capacitor error calibration, respectively. The proposed ADC is implemented using 180-nm CMOS technology in an area of 0.68mm^2. The calibration improves SNDR by 5.9 dB and SFDR by 14.3 dB, achieving an SNDR of 87.5 dB and an SFDR of 106.85 dB, respectively.**

Index Terms—**Analog-to-digital conversion (ADC), successive approximation register (SAR), calibration, high-resolution ADC**

I. INTRODUCTION

Successive approximation register (SAR) ADC has been the most preferred candidate in low-power sensor applications [1-5]. Though it can provide a burst-mode conversion for the duty-cycled system with superior energy efficiency, achievable effective number of bits (ENOBs) are limited to 10~11b. For sensor applications requiring an ENOB of over 14b, oversampling ADCs using delta-sigma modulators (DSMs) [7-10] have been general candidates, but at the cost of more energy consumption. To mitigate the problem of comparator noise in SAR ADC, two-step pipe-lined-SAR architecture with a gain stage between two SAR steps has been actively investigated [6]. However, the mismatch among capacitors and tightened requirement of high-precision analog circuits for inter-stage processing eventually limit the maximum achievable ENOBs.

Residue-integration (RI) SAR ADCs [11-13] have been also considered for fine-precision applications. Though they demonstrated effectiveness both in robustness against comparator noise and in energy efficiency, they require a high-gain amplifier for RI [11, 12]. In [13], combining a DSM in RI operation helps to relieve the constraint on the amplifier gain. Though it reduces the requirement of high-precision analog circuits, mismatch among capacitors is still left to be the performance-limiting factor. Adopting dynamic element matching (DEM) can reduce the effect of capacitor mismatch. However, applying DEM brings about complicated circuit blocks and is limited to only a part of capacitor bank of SAR ADC [13, 14].

The calibration technique has been considered to compensate for capacitor mismatches, hence improving the code linearity [15-20]. The effect of capacitor mismatch could be also reduced by employing a redundancy [15], but at the cost of complicated processing of sub-2 radix-based conversion. As an alternative approach, background calibration schemes [16-20] have been actively investigated. However, they cause complicated digital logic and require a long time with a wide-range of input to collect sufficient statistical information for the calibration.

This paper presents a digital-domain capacitor

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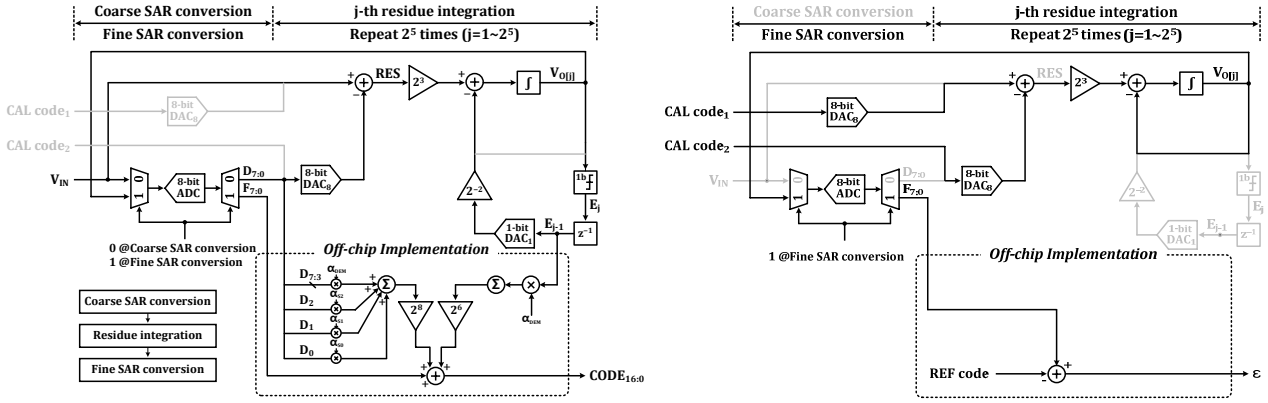
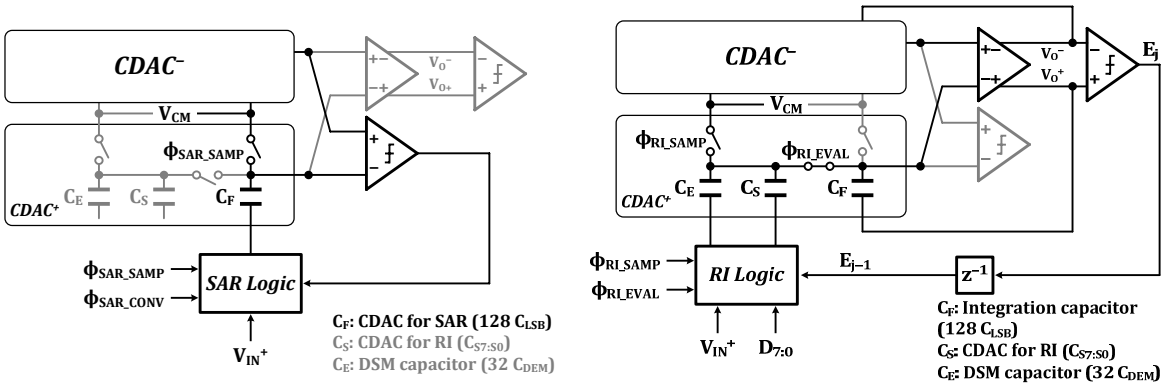


(a) (b)

Fig. 1. Architecture of the proposed SAR ADC in (a) conversion mode, (b) calibration mode.



(a) (b)

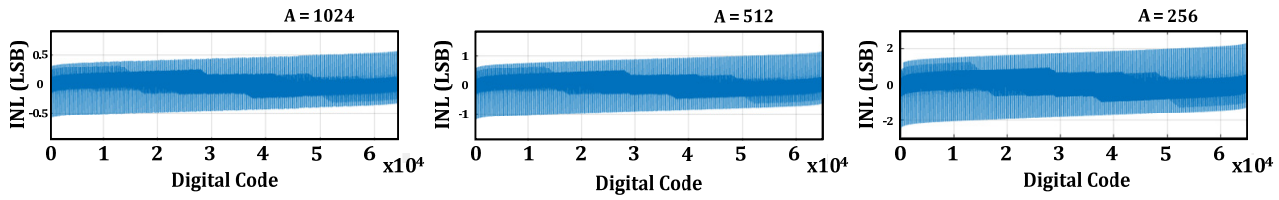
Fig. 2. Circuit configurations in the conversion mode for (a) coarse/find SAR conversion, (b) residue integration.

mismatch calibration scheme in RI SAR ADC. For verification, a 16-bit ADC is implemented in 180 nm CMOS technology, achieving an SNDR of 87.50-dB, an ENOB of 14.24b, and an SFDR of 106.85-dB. Section 2 describes the circuit and algorithm for the calibration. Section 3 shows measurement results, and Section 4 concludes this work.

II. CIRCUIT DESCRIPTION

1. Architecture

The designed ADC is based on [13], operating with two modes, conversion mode and calibration mode (Fig. 1). In the conversion mode, ADC receives the analog input V_{IN} and quickly performs 8-bit asynchronous SAR conversion, generating coarse 8 MSBs. Then, the residue integration is performed while receiving V_{IN}. It accumulates the quantization error by estimating V_{IN} with the coarse 8 MSBs. After repeating the integration 2^5 times, the result is quickly converted again with the same SAR conversion used in the first step, generating fine 8 bits. During the residue integration step, a DSM loop simultaneously converts 1-bit output (E_j) in parallel at each of 2^5 integration cycles. It helps to confine the amount of integrated residue and greatly relieves the requirement of amplifier gain. The total sum of two SAR conversion outputs and DSM outputs becomes the final digital output. In the summing process, the 8-bit output of the first SAR conversion are scaled up by 2^8. Since each DSM output affects the residue with a significance of the 5th bit and the residue is then amplified by 2^3, the DSM output should be scaled by 2^{8-5+3}, or 2^6. Detailed circuit operation in the conversion mode is explained in



(a) (b) (c)

Fig. 3. Simulated INL with amplifier gain of (a) 1024, (b) 512, (c) 256.

Fig. 2. A DEM is applied to 5 MSB capacitors for averaging. The capacitors for 5 MSBs ($C_{S7:S3}$) are implemented in a segmented capacitor array with each capacitance of $32C_{DEM}$. The 31 capacitors of $C_{S7:S3}$ and a DSM capacitor (C_E) form 32 identical capacitors for DEM. The DEM rotates the role of each capacitor during one full conversion of 32 cycles.

The RI with DSM greatly relieves the required open-loop amplifier gain. Assuming that V_{DD} is the input conversion range, the maximum amplifier output ($V_{o,max}$) during RI process confined by DSM operation becomes

$$|V_{o,\max}| \le 2^{-5+3} \cdot V_{DD} = 2^{-2} \cdot V_{DD} \quad (1)$$

Therefore, the maximum nonzero difference at the amplifier input during RI process due to the finite amplifier gain, A, is

$$\frac{2^{-2} \cdot V_{DD}}{A} \quad (2)$$

which becomes the input-referred error at the amplifier input. Since the inter-stage closed-loop gain for the fine conversion can be reduced by the number of RI cycle (2^5), the maximum error at the amplifier output for the fine conversion is calculated to be

$$\frac{2^8}{2^5}\frac{2^{-2} \cdot V_{DD}}{A} \quad (3)$$

which should be less than 1 LSB of the 8-bit fine conversion, or $V_{DD}/2^8$. It leads to the requirement for A, as

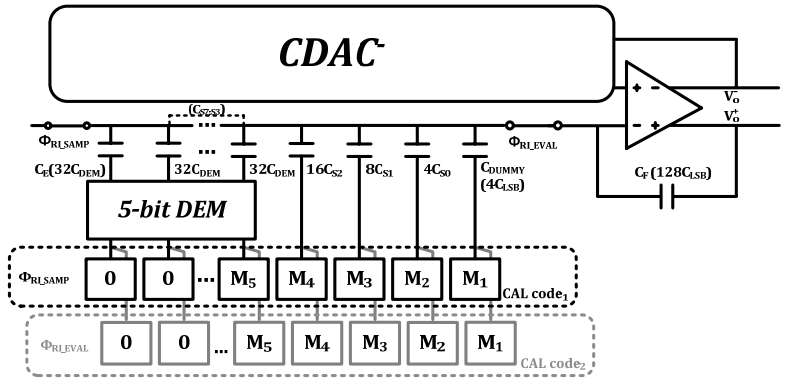
$$A > 512 \ (= 54.3 \text{ dB}) \quad (4)$$

Thus, the requirement for the amplifier gain is effectively reduced with factors of 2^{-2} and 2^{-5} by DSM and RI, respectively. Fig. 3 shows simulated INL for different amplifier gains, revealing the validity of the analysis.

In the calibration mode, a test input is self-generated by applying a known digital code. For the estimation of capacitor mismatch, two different combinations of digital codes representing the same amount of test input are prepared. Once the two digital codes are given, the residue integration is directly processed without the coarse conversion step. While one digital code provides an equivalent input, the other digital code performs the role of the coarse MSBs. The result of residue integrations is supposed to be 0 if the capacitors are perfectly matched. A nonzero residue is then converted through the subsequent fine SAR operation. Thus, the amount of capacitor mismatch among the sampling capacitors can be extracted from the ADC output code.

2. Calibration Algorithm

The calibration mode estimates the effect of mismatches of the eight MSB capacitors used for the input sampling during residue integration. The error is represented in a form of a ratio with the feedback capacitance ($128C_{LSB}$). Fig. 4 shows how to estimate the capacitance mismatch error. Let the dummy capacitor (C_{DUMMY}) of $4C_{LSB}$ be the reference. The capacitances, C_{LSB}, C_{S0}, C_{S1}, C_{S2} and C_{DEM} are identical if there is no error. To measure each capacitor error, two given calibration codes (CAL code$_1$, CAL code$_2$) are applied as the input and the estimated code for residue integration, respectively. The mismatch between $4C_{S0}$ and C_{DUMMY} leads to a nonzero residue at the amplifier output after the first cycle of the residue integration, which is



(a)

		M_5	M_4	M_3	M_2	M_1
ε_{S0}	CAL code$_1$	0	0	0	V_{REF}	0
	CAL code$_2$	0	0	0	0	V_{REF}
ε_{S1}	CAL code$_1$	0	0	V_{REF}	0	0
	CAL code$_2$	0	0	0	V_{REF}	V_{REF}
ε_{S2}	CAL code$_1$	0	V_{REF}	0	0	0
	CAL code$_2$	0	0	V_{REF}	V_{REF}	V_{REF}
ε_{DEM}	CAL code$_1$	V_{REF}	0	0	0	0
	CAL code$_2$	0	V_{REF}	V_{REF}	V_{REF}	V_{REF}

(b)

Fig. 4. (a) Circuit configurations, (b) code sets for estimation of capacitor mismatch in the calibration mode.

$$\begin{aligned} V_{O[1]} &= V_{O[1]}^{+} - V_{O[1]}^{-} \\ &= \left(\frac{4C_{S0}}{128C_{LSB}}(V_{REF} - 0) + \frac{4C_{LSB}}{128C_{LSB}}(0 - V_{REF}) \right) \\ &- \left(\frac{4C_{S0}}{128C_{LSB}}(0 - V_{REF}) + \frac{4C_{LSB}}{128C_{LSB}}(V_{REF} - 0) \right) \\ &= \frac{1}{16}\frac{C_{S0}}{C_{LSB}}V_{REF} - \frac{1}{16}V_{REF} \end{aligned} \tag{5}$$

After the 32nd integration, the output becomes

$$V_{o[32]} = 32V_{o[1]} = 32 \times \left(\frac{1}{16}\alpha_{S0} - \frac{1}{16} \right) V_{REF} \tag{6}$$

where $\alpha_{S0} = C_{S0} / C_{LSB}$. The α_{S0} becomes 1, or $V_{o[32]}$ is 0, if there is no mismatch error. Subsequent processing of $V_{o[32]}$ by the fine AD conversion reveals the information of mismatch error in a form of digital code. Defining ε_{S0} to be the mismatch error in the capacitor C_{S0},

$$\alpha_{S0} = 1 + \varepsilon_{S0} \tag{7}$$

The mismatch error for C_{S1}, represented by ε_{S1}, can be also derived in a similar way using the previously obtained ε_{S0}. Since the five MSB capacitors ($C_{S7:S3}$) and C_E are averaged by DEM, the mismatch error for those capacitors can be represented by a single parameter with an averaged error. The capacitance ratios can be obtained as follows:

$$\begin{aligned} \alpha_{S1} &= \frac{1}{2} + \frac{1}{2}\alpha_{S0} + \varepsilon_{S1} \\ \alpha_{S2} &= \frac{1}{4} + \frac{1}{2}\alpha_{S1} + \frac{1}{4}\alpha_{S0} + \varepsilon_{S2} \\ \alpha_{DEM} &= \frac{1}{8} + \frac{1}{2}\alpha_{S2} + \frac{1}{4}\alpha_{S1} + \frac{1}{8}\alpha_{S0} + \varepsilon_{DEM} \end{aligned} \tag{8}$$

where $\alpha_{DEM} = C_{DEM} / C_{LSB}$, $\alpha_{S2} = C_{S2} / C_{LSB}$ and $\alpha_{S1} = C_{S1} / C_{LSB}$. The mismatch errors for capacitors C_{S1}, C_{S2} and $C_{S7:S3}$ are represented by ε_{S1}, ε_{S2} and ε_{DEM}, respectively. The digitally estimated capacitance ratios (α_{DEM}, α_{S2}, α_{S1} and α_{S0}) are used in the conversion mode by multiplying α_{DEM} to $D_{7:3}$, α_{S2} to D_2, α_{S1} to D_1, α_{S0} to D_0 and α_{DEM} to $E_{31:0}$, respectively. These multiplications can be simply implemented by addition of binary-weighted digitized errors (ε_{S0}, ε_{S1}, ε_{S2} and ε_{DEM}).

To verify the calibration algorithm, we applied random mismatch to DAC which is comprised of unit capacitors. Fig. 5. shows simulated results when Gaussian statistics are applied to MSB capacitors with standard deviations of 0.02 and 0.05. The calibration noticeably improves linearity performance without any missing code. The conventional calibration schemes by only manipulating the final output code without affecting capacitor DAC could result in missing codes. However, the proposed calibration is applied to the coarse 8 bits and DSM bits before the summation with the fine 8 bits. Since the use of DSM provides a nonzero overlap between coarse 8 bits, there is no missing code in the calibrated output.

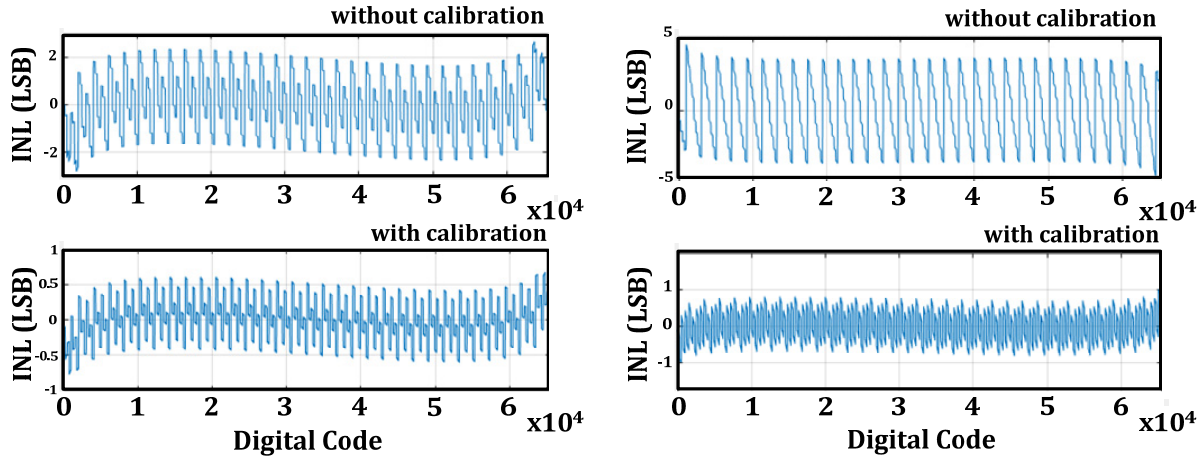


Fig. 5. Simulation results according to MSB capacitor mismatch applied to Gaussian statistics with standard deviation of (a) 0.02, (b) 0.05.

III. MEASUREMENT

The proposed ADC is fabricated using 180-nm CMOS technology, occupying a die area of 0.90 mm x 0.75 mm (0.68 mm^2). Fig. 6. shows a die photo. The unit capacitance is 20.28fF which is the smallest metal-insulator-metal (MIM) capacitor with the given technology. Using V_{DD} as V_{REF}, a full-scale differential input signal of $3.6V_{pp}$ is converted. The chip provides the outputs of the two SAR conversions and the DSM codes to off-chip program, so that the calibration is verified through software.

Fig. 7 shows fast Fourier transform (FFT) spectra with a low-frequency input. Without the calibration, SNDR performance is mainly limited by harmonics caused by capacitor mismatches. However, the calibration improves SNDR by 5.9 dB and SFDR by 14.3 dB, achieving 87.5 dB and 106.85 dB, respectively. It represents an ENOB of 14.24-bit. A near Nyquist-rate input shows an insignificant degradation of performance (Fig. 8). The effect of calibration is also seen in code linearity (Fig. 9). There are outstanding repeated 32 patterns in INL and DNL plots before calibration. It is due to capacitor mismatch between averaged DEM capacitance and other MSB capacitances. While the peak INL lies within +3.56/-3.36 without the calibration, it is improved to +2.14/-2.08 with the calibration. In the whole range of the input frequency, SNDR and SFDR are improved by calibration (Fig. 10). Table 1 summarizes and compares performance with previously reported SAR ADCs whose

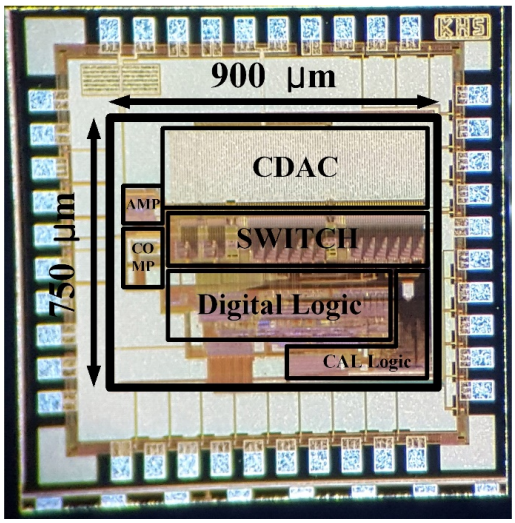
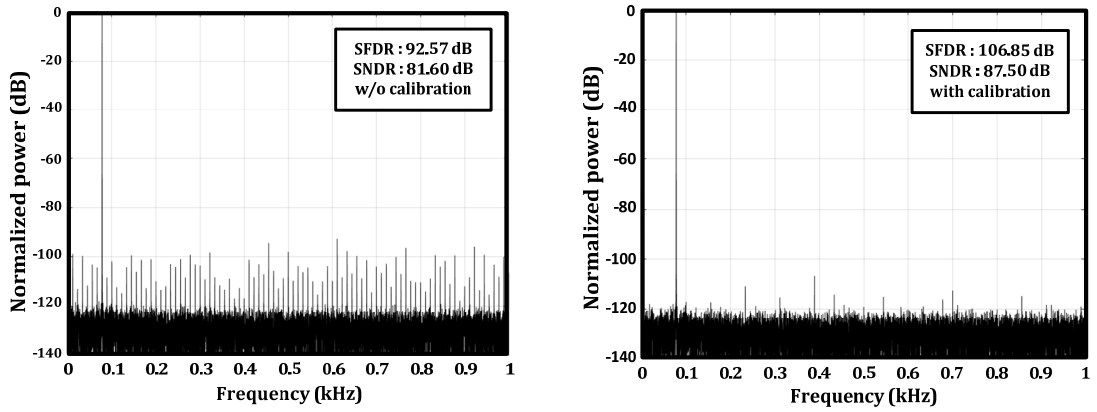


Fig. 6. Chip microphotograph.

resolution is higher than 12-bits. Since the final code is generated through software-based calibration, the total power consumption including digital-domain code scaling can be only expected by estimation. This work is continued research of [13] using the same core blocks. Additional power consumption for digital-domain code scaling at the output stage is estimated to be still negligible.

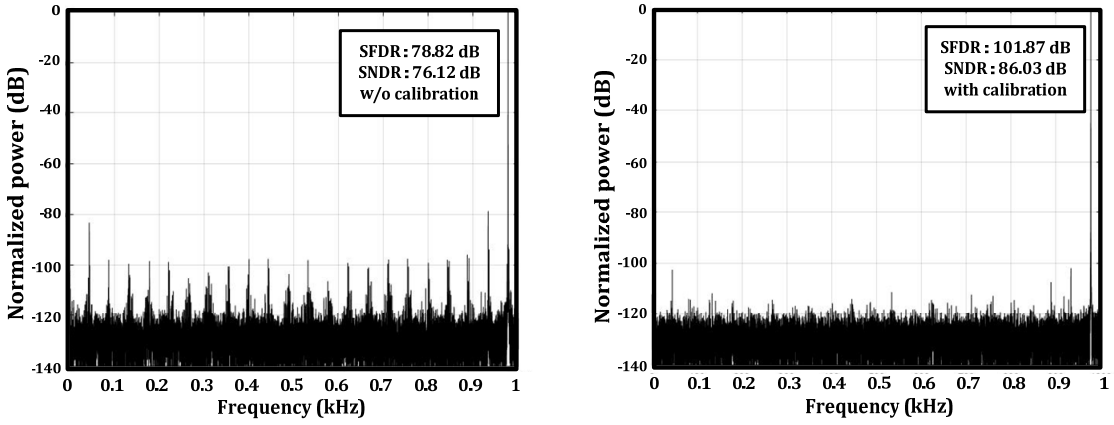
IV. CONCLUSIONS

This work proposes a capacitor mismatch calibration scheme for a residue-integrated SAR ADC. Unlike the conventional DSM-driven oversampling noise-shaping



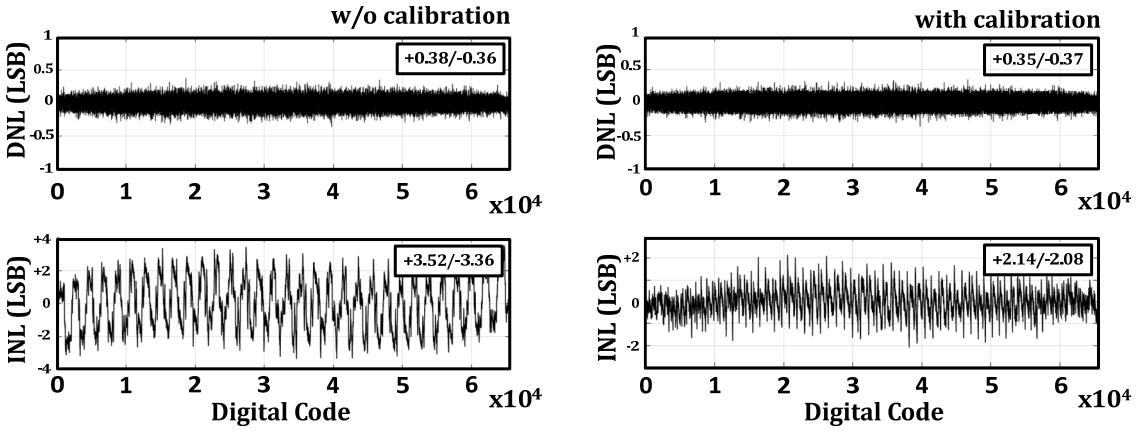
(a) (b)

Fig. 7. The 65536-point FFT spectra calculated from measurement at a low-frequency input (a) without calibration, (b) with calibration.



(a) (b)

Fig. 8. The 65536-point FFT spectra calculated from measurements at a near Nyquist-rate input (a) without calibration, (b) with calibration.



(a) (b)

Fig. 9. Measured code linearity (a) without calibration, (b) with calibration at sampling rate 2 kS/s.

Table 1. Performance Comparison with Nyquist-Rate ADCs

	This work	JSSC' 20 [22]	IEEE' 19 [21]	TCAS' 19 [5]	JSSC' 18 [13]	VLSI' 17 [17]	ISSCC' 17 [7]	VLSI' 16 [9]
Architecture	SAR	SAR	SAR	SAR	SAR	SAR	pipe. SAR	SAR
Technology [nm]	180	40	180	130	180	55	40	40
Resolution [bits]	16	13	16	12	16	16	14	15
Area [mm^2]	0.68	0.005	5.61	0.16	0.68	0.55	0.342	0.32
f_s [kS/s]	2	40k	1000	1	2	16k	35k	20
Power Supply [V]	1.8	1.1	5	1	1.8	5/2.5	-	-
Power [μW]	8.1*	591	40k	0.11	7.93	10.5k	21.8k	1.17
$SFDR_{Nyquist}$ [dB]	106.85	79.2	107.9	78.5	98.2	82	94.3	95.1
$SNDR_{Nyquist}$ [dB]	87.5	69	92.3	64.8	84.6	80**	75.1	74.1
FOMs [dB]	168.4*	174.3	166.3	161.4	165.6	165**	164.1	173.4

* : expected
** : with low frequency input
FOMs = SNDR + 10·log(BW/Power)

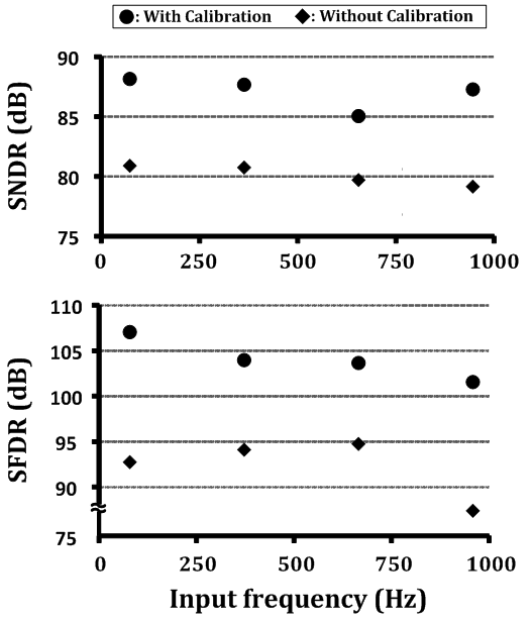


Fig. 10. SNDR and SFDR vs. input frequency according to use of calibration at sampling rate 2 kS/s.

ADC, the proposed ADC does not require any extra post-processing for decimation or filtering while performing integration of residue for noise averaging. Matching error in the binary-weighted input-sampling capacitances is estimated in a form of a digital number which is used for the scaling of corresponding digital number which is used for the scaling of corresponding digital code at the output stage during conversion. A 16-bit ADC is implemented using 180-nm CMOS technology. The calibration achieves 87.5 dB SNDR and 106.85 dB SFDR, showing improvements of 5.9 dB and 14.3 dB respectively.

ACKNOWLEDGMENTS

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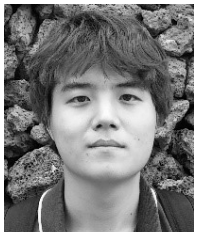

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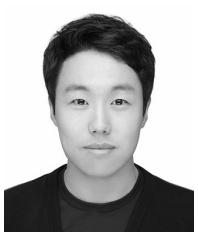

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