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12.2 GHz All-digital PLL with Pattern Memorizing Cells for Low Power/low Jitter using 65 nm CMOS Process

Sanggeun Lee and Taehyoun Oh*

***Abstract*—A system level power/jitter reduction technique of all-digital phase locked loop (ADPLL) design has been developed. The architecture to memorize the repetitive control signal pattern of digitally-controlled oscillator (DCO) during lock state and to regenerate the pattern, achieve the reduced power consumption compared to conventional mode from 14.4 mW to 9.51 mW in 1.0 V supply at 12.2 GHz and concurrently reduce jitter from 1.86 ps to 1.56 ps. The prototype PLL has been fabricated in 65 nm CMOS process and occupies 0.16 mm^2 chip area.**

***Index Terms*—PLL, digital PLL, frequency control word, pattern memory**

I. INTRODUCTION

Low jitter performance of clock sources (PLL) critically constrains the achievable operation speed of sub-triggered digital blocks in over 10 Gbit/s serial links. The circuit blocks operating at this speed usually consume several mW level power to support sufficiently steep signal transition. LC oscillators have been known to be superior in phase noise performance compared to ring oscillators but tuning range and area should be traded-off. Circuit level techniques such as current reused oscillator improve power consumption with wide frequency operation [1]. Linearizing Kvco by discrete capacitor bank (instead of varactors) contributes to jitter reduction performance [2]. Replacing non-linear varactors with tuned back gate of negative-Gm MOSFETs, makes possible low power and wide tuning range operations [3]. Most researches related to power and jitter reduction in clock generation circuits have been focused on block level techniques. In this paper, we propose a system-level pattern-memorizing clock generation techniques to reduce power and jitter for the first time to our best knowledge. From the insight that the

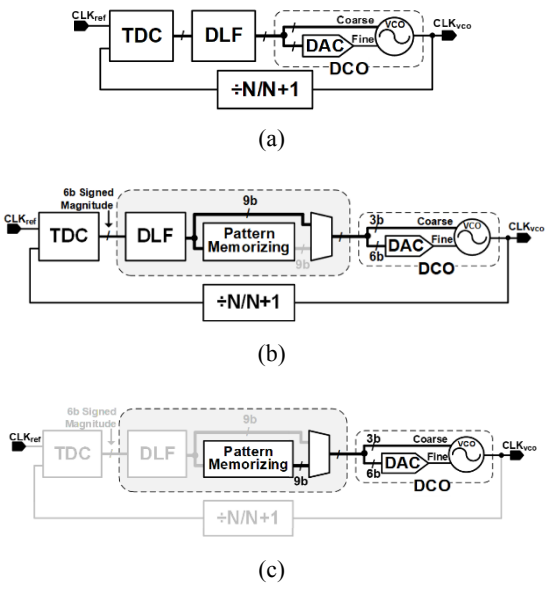

Fig. 1. Description of the ADPLL architectures (a) Conventional ADPLL, (b) Proposed PM-ADPLL in ordinary loop (OL) mode, (c) Proposed PM-ADPLL in pattern regeneration (PR) mode.

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Department of Electronic Engineering, Kwangwoon University, 615, Bima build., 20, Gwangun-ro, Nowon-gu, Seoul 139-701, Korea
E-mail : ohtaehyoun@kw.ac.kr

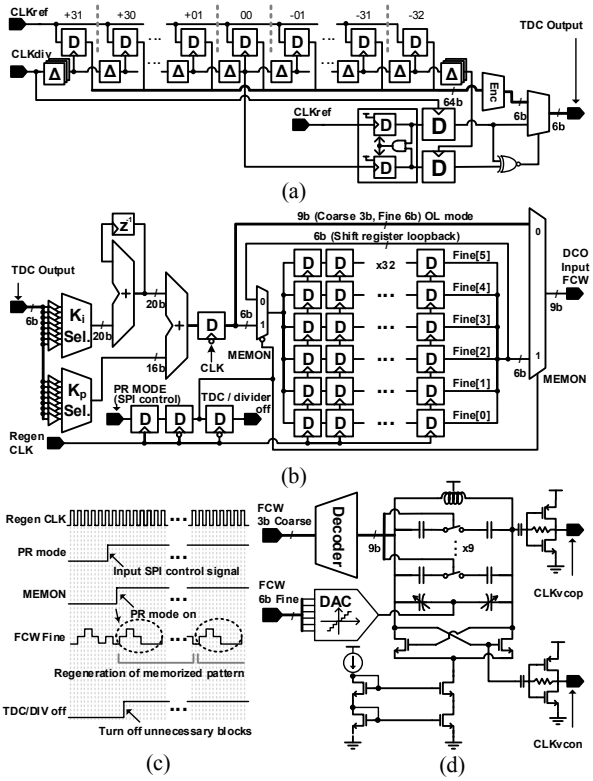

Fig. 2. Detail circuit diagrams of proposed PM-ADPLL (a) TDC schematic, (b) Proposed DLF and PM schematic, (c) Timing diagram of PM block for mode change, (d) LC-DCO and level shifter (LS) schematic.

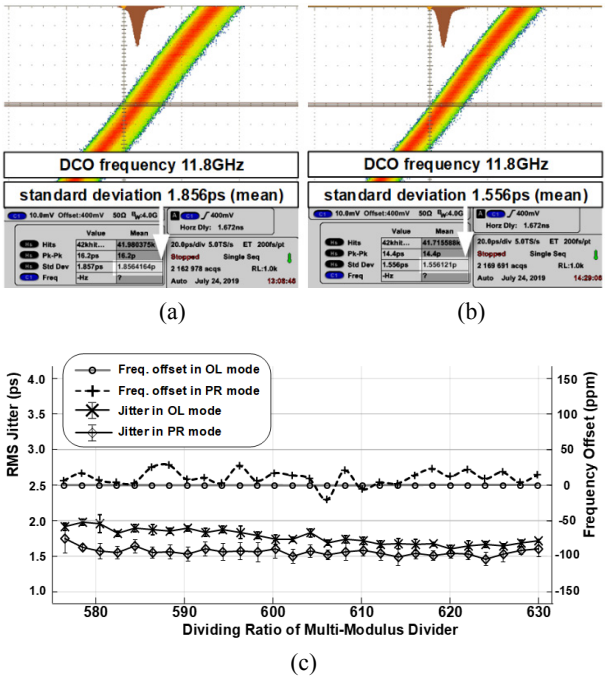

Fig. 3. Measurement comparison of OL mode and PR mode (a) RMS jitter(ps) when N=590 (OL mode), (b) RMS jitter(ps) when N=590 (PR mode), (c) VCO output frequency and RMS jitter comparison for both modes.

control signal of the oscillator in the loop shows a repetitive pattern in a lock condition, we noticed that memorizing the pattern can obviate the need for running the whole feedback loop. The PLL can be applied to trigger a HDMI 2.1 full-rate wireline transmitter which meets maximum data rate of 12 Gbps/lane.

II. ARCHITECTURE

Fig. 1 shows the conventional ADPLL and proposed pattern-memorizing ADPLL (PM-ADPLL). Conventionally, the digital loop filter (DLF) integrates the phase difference signal in a digital format from the time-to-digital converter (TDC) and updates the input frequency control word (FCW) of the DCO, as shown in Fig. 1(a). To maintain the intended target frequency accurately at the DCO output (CLKvco), the whole negative feedback loop must be turned on in this scheme and the divider p-

art consumes mW level power where the current-mode logic (CML) latches operate at giga-hertz speed. In our PM-ADPLL, as shown in Fig. 1(b), we added the low speed / small area pattern memorizing (PM) block. During OL mode, the PM block memorizes the repeating FCW lock pattern which will result in the target DCO output frequency if regenerated. After switching to PR mode, as shown in Fig. 1(c), our PM-ADPLL regenerates the memorized pattern and the accurate DCO output frequency at the individual chip corner can be obtained without burning power of TDC, DLF and divider. Additionally, disabling these digital blocks has an advantage of reducing supply noise in a typical ADPLL, where the supply nodes of digital blocks and analog oscillator block are usually not separated in layout. During the PR mode, the low speed PM block is triggered by the reference clock source.

Fig. 2(a) shows our TDC. The Vernier-type TDC [4] transforms input phase difference with 29.7 ps time resolution into 6-bit digital signals. Fig. 2(b) shows the circuit diagram of the proposed DLF and PM block. Fig. 2(c) illustrates the signal waveforms for mode switching. The 6-bit TDC output signal passes through Ki path and Kp path with gain ranges of 2^{-4}~2^{-11} and 2^{0}~2^{-7} each respectively. The integrated 9-bit signals (3-bit for coarse control, 6-bit for fine control) are transferred to the DCO input node during OL mode. By designing the

overlapping frequency of DCO with sufficiently wide ranges, the 3-bit coarse control signal does not change after the loop lock but only the 6-bit fine control signal moves with a repetitive pattern. Therefore, the coarse control signal is shared for both modes to downsize the PM block and the repeated fine control signal keeps being updated in the 32×6-bit shift register. When the PR MODE signal is switched on, the MEMON node becomes 1 and the 6-bit loopback path of shift registers are enabled. The DCO input node starts to get its fine control signal from the repeated shift register pattern. After one clock cycle, the TDC/divider blocks are turned off. The DLF input signal does not move in turn and the block is powered down. During PR mode operation, the output of PLL contains spur originates from a period of regenerated FCW pattern which has frequency of reference clock frequency divided by the pattern memory length. The 20 MHz reference clock frequency with 32-bit pattern memory generates 625 kHz spur. When the source clock from the proposed PLL is used to trigger the wireline transceiver with an operation frequency of 12 Gbps, the spur frequency is thousand times lower than the operation frequency of data recovery (CDR) and the jitter can be tracked readily [5]. Fig. 2(d) illustrates the schematic diagram of LC-DCO/LS and the bias is brought down to half of supply via LS. The power of following CML divider amount to mW level to support the speed.

III. Measurement Results

Fig. 3(a) and (b) shows the jitter measurement comparison of OL mode and PR mode at 11.8 GHz DCO output frequency divided by 20. To measure jitter, histogram box is used on rising edge after a period from trigger point of Tektronix DSA 70404. Over 41,000 samples on histogram box was measured and shown in Fig. 3(a) and (b) to achieve $\pm 0.0035\sigma_n$ error where σ_n is standard deviation. When the mode is switched from OL to PR, the root-mean-square (RMS) jitter is improved from 1.86 ps to 1.56 ps but the DCO output frequency does not change as intended. We estimate that the improvement comes from supply noise reduction when the digital blocks are turned off during PR mode. Fig. 3(c) presents the measured RMS jitter and DCO output frequency for both modes when the dividing ratio is

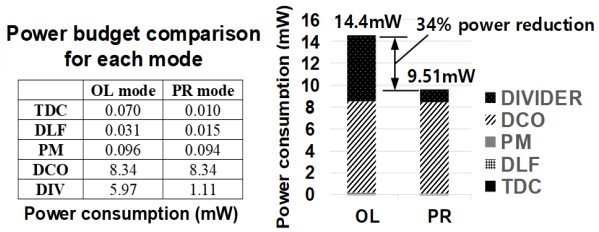

Fig. 4. Power budget of OL mode and PR mode.

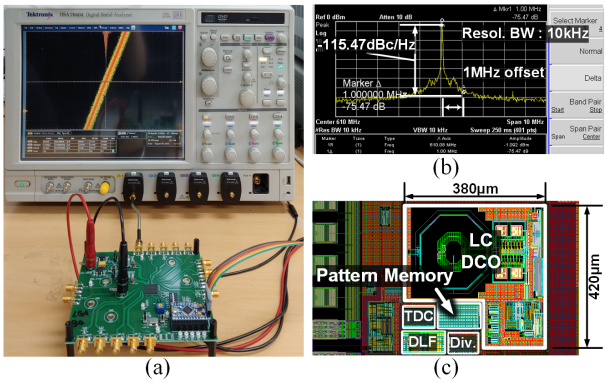

Fig. 5. Measurement setup and IP layout (a) Measurement environment (Tektronix DSA 70404), (b) Phase noise measurement with spectrum analyzer (HP E4401B), (c) Layout.

Table 1. Comparison Table

		[6]	[7]	This Work
Technology		90nm	40nm	65nm
Area (mm^2)		1.2	0.32	0.16
Center frequency (GHz)		-	-	12.2
Frequency Tuning Range (GHz)		9.2-12	11.7-13.5	11.52-12.6
Power (mW)	OL mode	50	33.8	14.4
	PR mode	-	-	9.51
RMS Jitter (ps)	OL mode	-	-	1.856
	PR mode	-	-	1.556
Phase Noise @1MHz (dBc/Hz)		-112.3	-97.3	-115.47 (PR mode)
FOM_T (dBc/Hz)		-184.25	-167.12	-186.4
※$FOM_T=L(\Delta f)-20\log(f_0/\Delta f)+10\log(P_{DC}/1mW)-20\log(FTR/10\%)$				

swept from N=576 to N=630 by setting up the sweep measurement via general purpose interface bus (GPIB) interface with Tektronix DSA70404. Overall RMS jitter for all frequency range is improved by 0.212 ps on average while DCO output frequency stays within ±13 ppm (avg.) range. The measurement result during OL mode shows -52.85 dBc of reference spur at 20 MHz. After transition to the PR mode, the PLL does not have noise immunity provided by the OL mode. The PLL

needs to be updated by turning on the OL mode every once in a while maintaining the lock. Fig. 4 presents power consumption of each block in both OL mode and PR mode with 1.0 V supply voltage. By turning off the giga-hertz speed divider, 4.9 mW can be saved. Fig. 5(a) shows the picture of experiment environment and Fig. 5(b) shows the measured phase noise (PN) in spectrum analyzer HP E4401B. The noise is measured after the clock signal at the DCO output is divided by 20. Our intellectual property (IP) has been fabricated in 65nm CMOS process and occupies 0.16 mm^2 die area, as shown in layout of Fig. 5(c).

The size of the PM block is 0.0094 mm^2 (only 5.9% of total PM-ADPLL size). Table 1 summarizes the performances of our IP and compares them to prior arts with similar applications. By turning on the PR mode, the power can be saved by 34% and the jitter is improved by 12% but the DCO output frequency is maintained accurately even after the mode is switched. The relatively lower tuning range is due to the design to achieve sufficiently wide overlapping frequency to avoid any blind frequency band during coarse control transition.

IV. CONCLUSIONS

A systematic pattern memorizing technique has been developed and applied to ADPLL successfully. The prototype chip has been fabricated in 65 nm CMOS process and its performances are compared to the works in similar applications. The measurement results show significant power and jitter reduction when the pattern regeneration mode is turned on.

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Sanggeun Lee received the B.S. degree in the department of electronic engineering from Kwang woon university, Korea, in 2020. He is currently pursuing the M.S. degree in Kwangwoon university, Korea. His research interests include PLL, clock recovery and high-speed IO circuits.

Taehyoun Oh (S'05) received the Bachelor of Science (B.S.) and Master of Science (M.S.) degrees in Electrical Engineering from Seoul National University in 2005 and 2007, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Minnesota, Minneapolis under the supervision of Dr. Ramesh Harjani. His doctoral research is focused on high-speed I/O circuits and architectures. During the summer of 2010, he worked on I/O channel modeling at AMD Boston Design Center, MA. In the fall semester of 2011, he researched on I/O architecture and jitter budgeting of the link at Intel Corp., CA. From fall of 2012, he joined the IBM system technology group, NY. and worked on performance verification of high-speed decision feedback equalizer for server processors. Since spring of 2013, he joined at the department of electronic engineering in Kwangwoon university in Seoul, Korea as an assistant professor. His current research interest is focused on clock generation IC design.