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Effects of Ultrasonication on the Electrical Performance of a-IGZO TFTs

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***Abstract*—In this study, investigate the effect of ultrasonication on the oxide channel layer of amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) based on different processing times. The ultrasonication treatment was applied at 40 kHz for 0, 10, 20, and 40 min before post annealing. Ultrasonication improved the electrical and surface morphology properties of a-IGZO thin-film transistors. The a-IGZO TFTs that underwent ultrasonication for 10 min exhibited enhanced electrical performance (saturation mobilities of 11.9 cm^2/Vs, current on/off ratio of 3.5×10^7, threshold voltage of 6.1 V, and subthreshold voltage of 0.65 V/dec). Moreover, the dynamic and static responses of a resistive load–type inverter based on a-IGZO with ultrasonication are examined.**

***Index Terms*—a-IGZO, oxide, thin-film transistor, sonication, morphology**

I. INTRODUCTION

With the rapid development of the display industry, heavy displays have been gradually replaced by flat and flexible displays. Therefore, high performance, low power, and large area display semiconductors are required in the next-generation semiconductor market [1-6]. Amorphous silicon (a-Si) transistor has been used as a switching device for most displays; however, its carrier mobility is insufficient to satisfy the essential requirements for high-performance and large-area displays. Hence, oxide semiconductors with high carrier mobility and excellent electrical stability have attracted attention [7-11]. Thin-film transistors (TFTs) based on oxide semiconductors can be processed at lower temperatures than transistors based on a-Si or low-temperature polycrystalline silicon, and they have higher reliability. Oxide semiconductors that have been investigated recently include zinc oxide (ZnO), tin monoxide (SnO), indium oxide (InO), indium zinc oxide (IZO), zinc tin oxide (ZTO), and indium–gallium–zinc oxide (IGZO). Most of them have been studied as devices for display backplanes [12-15].

Among them, amorphous IGZO (a-IGZO) has higher electron mobility than a-Si due to its high bandgap energy. It has better uniformity than polycrystalline silicon TFTs, and favorable for large area driving devices. Furthermore, it can miniaturize TFT circuits, and many studies have been conducted regarding its application in large-area and flexible displays because of its high optical transmittance [16-20]. As the size of display pixels decreases, the size of transistors for backplanes must be reduced correspondingly. Therefore, studies have been actively conducted to improve the carrier mobility of transistors based on an a-IGZO channel layer. Thus far, the electrical properties and performance have been evaluated under various processing conditions, such as different transistor structures, reduced contact resistance between the insulating and semiconductor channel layers, and different thicknesses for the

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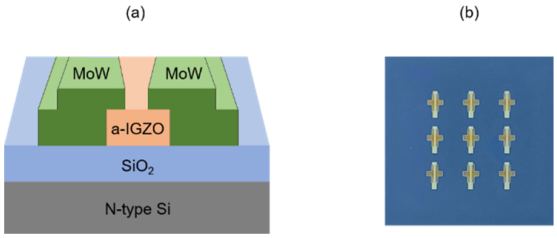

Fig. 1. (a) schematic diagram of a-IGZO TFT, (b) optical microscopy image of a-IGZO TFTs.

insulating and channel layers [21-28]. However, structure change or channel width reduction to improve carrier mobility is limited by physical restrictions and involves more processing steps. Therefore, studies regarding plasma, thermal, and sonication treatments on the a-IGZO channel layer have been conducted [29-34]. Among them, sonication is required to process nano-sized materials. It enables powerful particle removal and multidirectional treatment using the cavitation phenomenon and affords high penetration in a narrow space [35-37].

This study analyzes the effect of ultrasonication (when applied to the a-IGZO channel layer) on the electrical performance of TFTs based on treatment time. A gate bias stress (GBS) test was conducted to evaluate the reliability of a-IGZO TFTs based on ultrasonication against a continuous external voltage, and a resistive load–type inverter was constructed to observe dynamic and static responses for digital logic device applications.

II. EXPERIMENT

Fig. 1(a) is the schematic of a-IGZO channel layer–based TFT with a metal–insulator–metal structure, and Fig. 1(b) is an optical microscopy image of a-IGZO TFTs. A 100 nm thick layer of silicon dioxide (SiO_2) was grown by thermal oxidation on heavily doped n-type Si (600 um) wafer to serve as the gate dielectric. Subsequently, to remove impurities remaining on the surface, the substrate was subjected to piranha cleaning by immersing them in a sulfuric peroxide solution of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) mixed at a 3:1 ratio, followed by heating at 60 °C. Subsequently, sputtering was performed using a DC/RF magnetron sputtering system to deposit the a-IGZO channel layer.

In this study, argon (an inert gas) was used to achieve a smooth sputtering process, and a 1:1:1 a-IGZO (In_2O_3:Ga_2O_3:ZnO) target of diameter three inches attached to a gun-type plasma cell was used as the RF sputtering target. The RF power generator was set to 150 W, and sputtering was performed for 6 min 40 s, to deposit a 50 nm a-IGZO channel layer.

After deposition of the a-IGZO channel layer from sputtering, ultrasonication was applied to the a-IGZO channel layer thin-film surface at 40 kHz for 0, 10, 20, and 40 min using ultrasonication surface treatment equipment. Upon completion of the sonication process, the annealing process was performed to increase the electrical properties of the a-IGZO TFTs [38, 39]. The annealing process was applied at 350 °C for one hour after an air atmosphere was generated inside a box furnace. Upon completion of the post annealing process, channels with a length of approximately 200 μm and a width of 2,000 μm were formed by depositing 100 nm molybdenum tungsten (MoW) source/drain contact electrodes using the DC/RF magnetron sputtering system.

To analyze the performance of the TFTs, their electrical performance and stability were evaluated in a darkroom under air atmosphere using a Keithley 2636 semiconductor parameter analyzer. In addition, changes in the a-IGZO channel layer based on the length of the ultrasonication process were analyzed using scanning electron microscopy (SEM). To evaluate the current of the fabricated TFTs over time and their stability according to the accumulated time of voltage application, current stress measurement and GBS tests were conducted using a Keithley 4200 semiconductor parameter analyzer. In addition, a resistive load type inverter circuit with a resistance of 1 MΩ was constructed to analyze device switching characteristics.

III. RESULTS AND DISCUSSION

In this study, ultrasonication was applied to the a-IGZO channel layer for different periods of time before annealing, and the optimal sonication time to improve the electrical and surface morphology properties of the a-IGZO TFTs was investigated. Fig. 2 shows the output curves of the as-deposited (as-dep) a-IGZO TFT and a-IGZO TFTs subjected to ultrasonication for 10, 20, and 40 min. V_{ds} was increased from 0 V to 30 V in 0.5 V

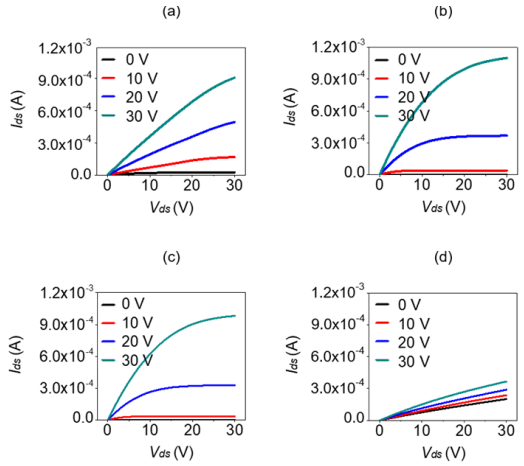

Fig. 2. Output characteristics I_{ds} - V_{ds} curves at four different V_{gs} levels in TFTs with a-IGZO channel layers treated with ultrasonication for different lengths of time (a) as-dep, (b) 10 min, (c) 20 min, (d) 40 min.

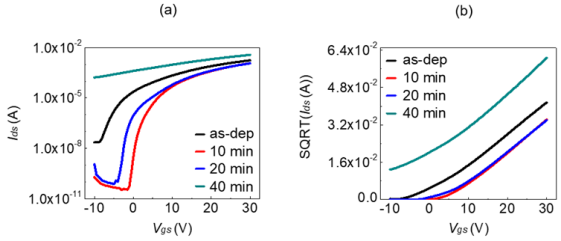

Fig. 3. Transfer characteristics I_{ds} - V_{gs} and square root I_{ds} - V_{gs} curves at V_{ds} = 30 V in TFTs with a-IGZO channel layers treated with ultrasonication for different lengths of time (a) transfer characteristics I_{ds} - V_{gs} curves, (b) square root I_{ds} - V_{gs} curves.

increments, and I_{ds} was measured under gate bias voltages of 0, 10, 20, and 30 V. In Fig. 2(b) and (c), the values at which the current output curves were saturated are high. This indicates that ultrasonication improved the electrical performance by removing impurities from the surface of the a-IGZO channel layer. In Fig. 2(d), however, the output curve is not saturated, compared with other devices, and no significant differences in I_{ds} are observed between the different gate bias voltages. This shows that excessive ultrasonication time degrades the performance of a TFT with an a-IGZO channel layer.

Fig. 3 shows the transfer curves of the as-dep a-IGZO TFT and a-IGZO TFTs subjected to ultrasonication for 10, 20, and 40 min. The graphs show the values of I_{ds} and the square root of I_{ds} when V_{gs} was swept from –10 to 30 V in 0.5 V increments with a 30 V drain bias voltage applied. The electrical properties of the devices were extracted based on the transfer curves, and the results are summarized in Table 1.

Table 1. Summary of Electrical properties of a-IGZO channel layers treated with ultra-sonication by different of time including μ_{sat}, I_{on}/I_{off}, V_{th}, S/S

Ultrasonication time	μ_{sat} (cm^2/Vs)	I_{on}/I_{off}	V_{th} (V)	S/S (V/dec)
As-dep	11.27	7.6×10^4	- 0.07	1.73
10 min	11.90	3.5×10^7	6.10	0.65
20 min	10.79	1.6×10^7	5.07	0.72
40 min	15.40	2.2×10^1	- 7.22	22.87

The a-IGZO TFTs subjected to ultrasonication exhibited higher carrier mobility and higher on/off current ratios (I_{on}/I_{off}) than the as-dep a-IGZO TFT, and the subthreshold swing (S/S) value improved. In the a-IGZO TFTs subjected to ultrasonication for 10 and 20 min, the I_{on}/I_{off} value increased by approximately 10^3 times owing to leakage current improvement. The S/S values of the transfer curves were more linear, compared with the as-dep a-IGZO TFT, and the on-current voltage exhibited a positive shift near 0 V. In the device subjected to ultrasonication for 10 min the carrier mobility increased slightly, and the S/S value improved. When the device was subjected to ultrasonication for 40 min, however, I_{on}/I_{off}, the threshold voltage (V_{th}), and the S/S value degraded significantly, compared with the as-dep a-IGZO TFT (even though its carrier mobility increased), and the shape of the transfer curve was not observed. It appears that ultrasonication improved the electrical performance of the a-IGZO channel layer-based TFTs by increasing the carrier mobility, as shown by the results in Fig. 2, and it was confirmed that the accumulation of the ultrasonication time increased the drain off-current, thereby significantly lowering the I_{on}/I_{off} value.

To investigate changes in the a-IGZO channel layer based on the length of ultrasonication treatment, the microstructure of the layer was analyzed using SEM.

Fig. 4 shows SEM images of the surface of a-IGZO channel layers treated with ultrasonication for different lengths of time. To capture images of the a-IGZO channel layers using SEM, a-IGZO TFT devices attached to sample plates using carbon tape were loaded into a vacuum, and the images were captured at 50,000 times magnification, while 1.0 kV of electron high tension was applied at a working distance of 2.5 nm. Fig. 4(b) shows

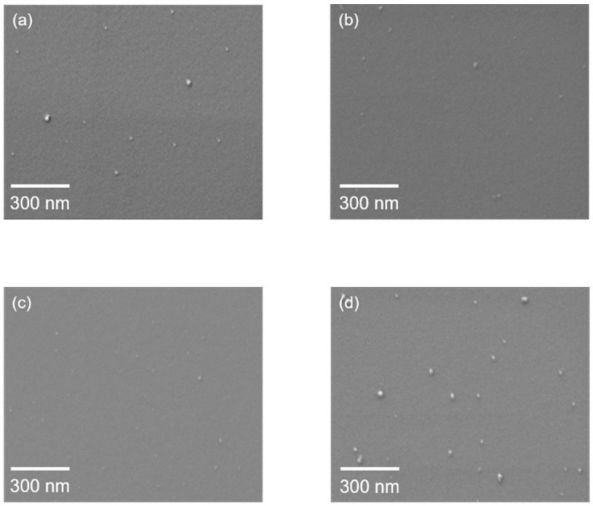

Fig. 4. Surface SEM images of a-IGZO channel layers treated with ultrasonication for different lengths of time (a) as-dep, (b) 10 min, (c) 20 min, (d) 40 min.

a uniform and smooth surface compared with that of the as-dep a-IGZO TFT. As shown in Fig. 4(c), the surface is smooth compared to the as-dep a-IGZO TFT, but irregular impurities are observed on the surface. As shown in Fig. 4(d), the surface is extremely irregular, and large impurities are observed, compared with those observed on other devices. Analysis of the a-IGZO channel layer revealed that the ultrasonication process generated a smooth surface by removing impurities from the film surface. This was because the free volume area, which is the empty space between molecules, was reduced as the irregular atomic arrangement of the amorphous material was rearranged through ultrasonication [40-42]. After long application of ultrasonication, however, the surface of the a-IGZO channel layer became rougher, and impurities were more visible. This is because the surface of the a-IGZO channel layer was eroded due to the accumulated sonication energy.

To evaluate the current stress of the a-IGZO TFTs based on the length of ultrasonication, and their stability according to the accumulated time of voltage application, current stability, positive bias stability (PBS), and negative bias stability (NBS) tests were conducted.

Fig. 5 shows the current stress measurement results from evaluating the reliability of the as-dep a-IGZO TFT and the a-IGZO TFTs treated with ultrasonication for 10 and 20 min. The ratio of I_{ds} (measured over time) to I_{ds0}, which was the initial measurement, was shown when

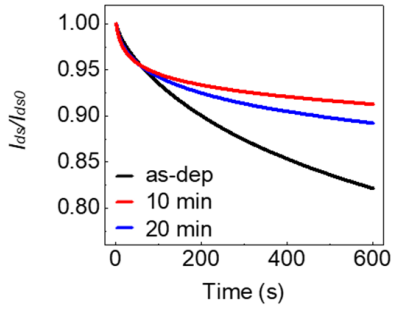

Fig. 5. Current stress characteristic curves for TFTs with a-IGZO channel layers treated with ultrasonication for different lengths of time: as-dep, 10 min, and 20 min (V_{ds} = 30 V, V_{gs} = 30 V).

30 V was applied as V_{gs} and V_{ds} for 10 min. For the device without ultrasonication, the current decreased rapidly over time. For the a-IGZO TFT treated with ultrasonication for 10 min, however, more than 90 % of the current was retained even after 10 min.

Fig. 6 and 7 show the gate bias stress stability of the as-dep a-IGZO TFT and a-IGZO TFTs treated with ultrasonication for 10 and 20 min. Fig. 6 shows the results of the PBS test, in which a positive voltage was continuously applied to the gate. In the test, 20 V was used, and the transfer curve was measured based on the application time. For the TFTs to be turned on or off, a positive or negative voltage must be applied to each circuit, respectively. When a positive or negative voltage is continuously applied to the gate, the electrons or holes in the channel layer are reduced as they are trapped at the interface between the insulating layer and the channel layer by electric force, and V_{th} increases or decreases depending on the applied voltage. If V_{th} does not exhibit a positive shift according to the positive voltage stress time when a positive voltage is applied in the PBS test, it can be assumed that the device is stable, which is a reliability evaluation index in this study. As shown in Fig. 6(b), different positive voltage stress times caused little change in the transfer curve. The figure shows the results of applying ultrasonication to the a-IGZO channel layer for 10 min. We discovered that the stability of the electrical properties improved.

Fig. 7 shows the results of the NBS test, in which a negative voltage was continuously applied to the gate. In the NBS test, the stability the stability of the TFT was evaluated based on the distance traveled by the transfer curve of the device in the negative direction when a

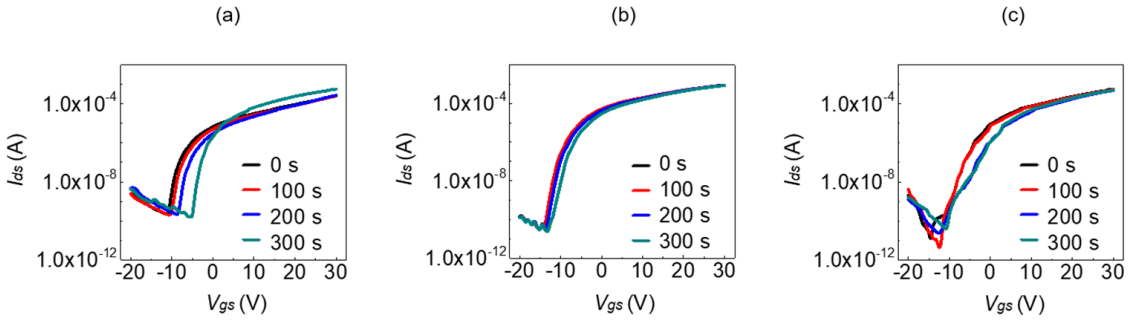

Fig. 6. Positive bias stress (PBS) stability of TFTs with a-IGZO channel layers treated with ultrasonication for different lengths of time (a) as-dep, (b) 10 min, (c) 20 min. The stress condition was V_{gs} = + 20 V.

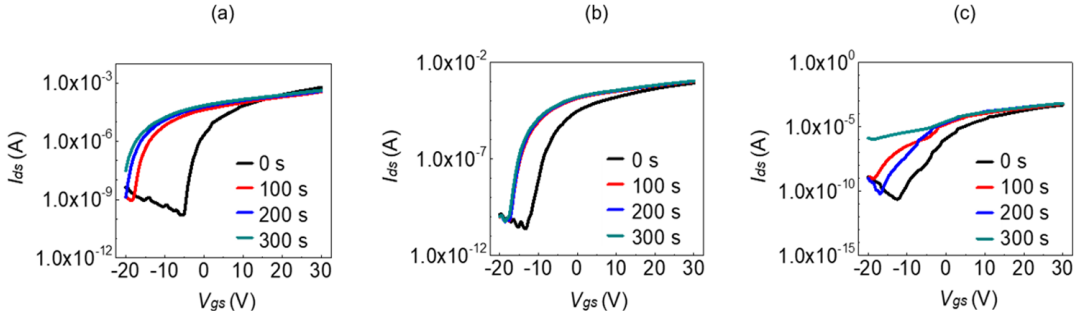

Fig. 7. Negative bias stress (NBS) stability of TFTs with a-IGZO channel layers treated with ultrasonication for different lengths of time (a) as-dep, (b) 10 min, (c) 20 min. The stress condition was V_{gs} = –20 V.

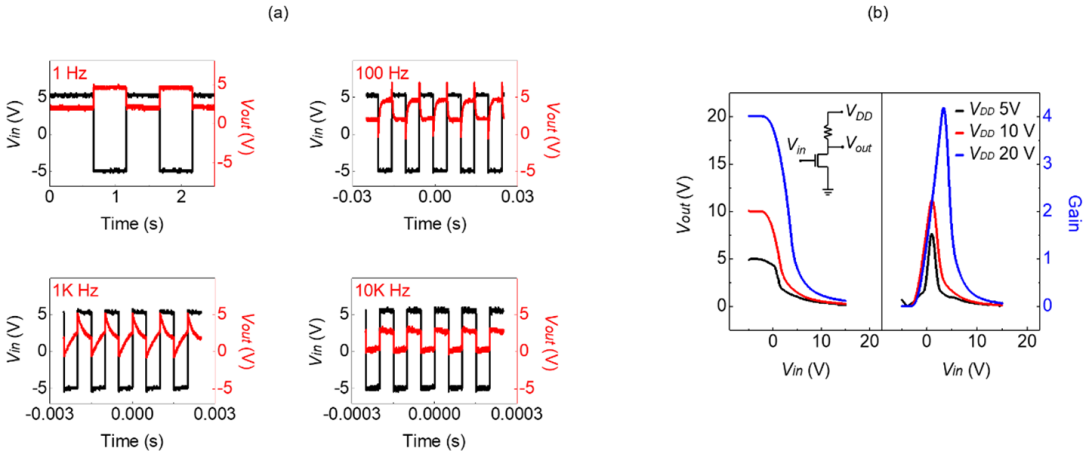

Fig. 8. Resistive load type inverter test by configuring the logic circuit for an a-IGZO channel layer based TFT treated with ultrasonication for 10 min (a) dynamic response characteristics based on 1 Hz, 100 Hz, 1 kHz, and 10 kHz (V_{DD} = 5 V, V_{in} = –5 V to 5 V); (b) results of the voltage transfer characteristic based on 5 V, 10 V, and 20 V V_{DD}.

negative bias voltage was applied to the device. In this study, –20 V was used, and the transfer curve was measured according to the application time. As the negative voltage stress time increased, V_{th} decreased, and I_{ds} increased. It was clear that V_{th} decreased as a small number of holes in the channel layer were injected into the gate insulator layer. In the device without ultrasonication, the transfer curve shifted significantly in the negative direction when a negative voltage was continuously applied for more than 100 s. In the TFT with the a-IGZO channel layer treated with ultrasonication for 10 min, however, the transfer curve did not exhibit a significant negative shift, resulting in excellent performance compared to the other two devices.

Based on the measurement results above, we discovered that ultrasonication before annealing improved the electrical and surface morphology properties of the a-IGZO channel layer-based TFTs, and the optimal ultrasonication treatment time is 10 min. Therefore, a resistive load type inverter test was conducted using the a-IGZO channel layer-based TFT treated with ultrasonication for 10 min, and the results are shown in Fig. 8. Fig. 8(a) shows the dynamic response characteristics according to the frequency measured using a power supply, an oscilloscope, and a function generator. The dynamic inverter test was conducted under different frequencies (1 Hz, 100 Hz, 1 kHz, and 10 kHz), while 10 MΩ was applied as the load resistance of the circuit, and 5 V as the drain supply voltage (V_{DD}). In the resistive-load-type inverter test, when V_{in} was -5 V, V_{out} was 5 V because the applied voltage was lower than V_{th}, which resulted in an opened infinite resistance among the gate, drain, and source. When 5 V was applied to V_{in}, however, V_{out} was 0 V, because a small resistance was generated among the gate, drain, and source, thereby allowing the current to flow to ground.

Fig. 8(b) shows the voltage transfer characteristics (VTC) measurement results for the a-IGZO device treated with ultrasonication for 10 minutes. The inset figure shows the inverter circuit composed of a semiconductor parameter analyzer and a source meter. As with the dynamic response characteristic circuit, 10 MΩ was applied as the load resistance, and V_{in} was increased from -10 to 20 V in 0.5 V increments. The VTC curve was measured when V_{DD} was 5, 10, and 20 V. The measured device exhibited the maximum gain value of 4.9306 when V_{DD} was 20 V. The dynamic response characteristic and VTC analysis results show that the a-IGZO channel layer-based TFT treated with ultrasonication for 10 min exhibited excellent inversion characteristics and sufficient response switching speed for the input square wave, thereby confirming its applicability as a device for display backplanes.

IV. CONCLUSIONS

To improve the electrical characteristics of a-IGZO TFT, a surface treatment of ultrasonication post annealing process was designed and applied to real experiment at room temperature under air environment. Ultrasonication was applied to the surface of the deposited a-IGZO channel layer at 40 kHz for 0, 10, 20, and 40 min. A semiconductor parameter analyzer and a scanning electron microscope were used to analyze changes in the electrical and surface morphology properties of the a-IGZO channel layer-based TFTs based on the length of sonication time.

The results indicated that the a-IGZO channel layer-based TFT treated with ultrasonication for 10 min exhibited excellent carrier mobility and I_{on}/I_{off} values, and its stable current and durability against external voltage were confirmed. The ultrasonication process generated clearer surface of the a-IGZO film and reduced the impurities, resulting in the reduced surface roughness. A long application of ultrasonication, however, generated clearer surface impurities and resulted in significantly degraded electrical performance. This implies that short sonication treatment improves the electrical and surface morphology properties, reducing defects by removing impurities from the surface of the a-IGZO channel layer and from atomic rearrangement; however, excessive sonication increased surface roughness by eroding the surface of the a-IGZO channel layer.

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