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Analytical Heat Transfer Model for a TTSVs-based Thermal Mitigation Power Chip

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***Abstract*—The work develops an analytical thermal model for a thermal Through Silicon Vias based heat mitigation power chip whose thermal path is quite different compared to the literatures published. Thermal spreading angle and transverse heat transfer of thermal Through Silicon Vias as well as its thermal stress impact on carrier mobility in active areas have been considered. Traditional one-dimensional thermal model used in three-dimensional integrated circuits and finite element analysis result are used to verify the accuracy of the proposed model. Temperature rise for the proposed structure with respect to the filling-via radius, bulk Si thickness, Through Silicon Via liner thickness and bonding layer thickness are investigated. It can be found that the proposed thermal model is superior than one-dimensional model in contrast with the simulation result which indicates an improvement in the thermal management of thermal Through Silicon Vias based three-dimensional integrated circuits associated with thermal-mechanical reliability.**

***Index Terms*—Through-silicon-via, thermal model, thermal-mechanical reliability, finite element analysis**

I. INTRODUCTION

Three-dimensional (3D) integration gains more and more attention for its advances in high density integration, low power consuming, low signal delay and thus improved frequency performance [1, 2]. However, thermal issues are becoming critical for the reliability of the whole electronic system resulting from the 3D stacked structure which increases the power density [3-5]. Through Silicon Vias (TSVs) inserting is proved to be an efficient method to mitigate the thermal problems for the high thermal conductivity of the Cu pillar inside a TSV structure experimentally [6]. In a 3D stacked system, heat flows across different materials with disparate thermal properties which return makes the thermal path and the calculation of thermal resistance much more complicated. For simplicity, many publications only take vertical resistance (1D resistance in z-direction) into considerations to give a first insight of the thermal performance of 3D integrated systems and easily estimate the thermal management requirements [7-9]. Though lateral thermal resistance is also considered [10-12], this kind of result is based on specific conditions that the heat source is perpendicular to the TSVs which is not usually the case in reality. Recently, the thermal resistance of a 3D laminated packaging structure is given based on simulation results but lacking of detailed physical derivations which is not suitable for the guidance of thermal management in 3D integrated systems [13]. Due to the obvious coeffcients of thermal expansion (CTE) mismatch between the Si and filled-in-via materials, the resulting thermal stress could degrade the chip performance under thermal cycling, because the carrier mobility has been changed [14-16] and certain

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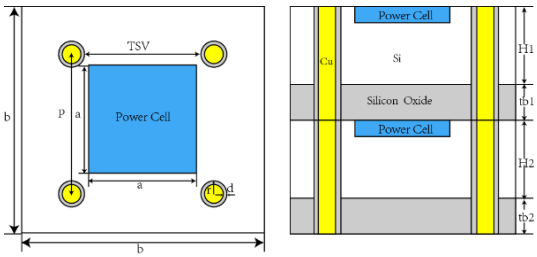


Fig. 1. Top view and cross section view of the power chip with TTSVs. The width and length of a power cell and bulk Si is a and b, respectively. And the distance between the nearest neighbor two TSVs is noted as P. The height of bulk Si and bonding layer in the 1st and 2nd layer is H1 and tb1, H2 and tb2, respectively. Parameters r, d is the radius of TSV, SiO_2 liner thickness, respectively.

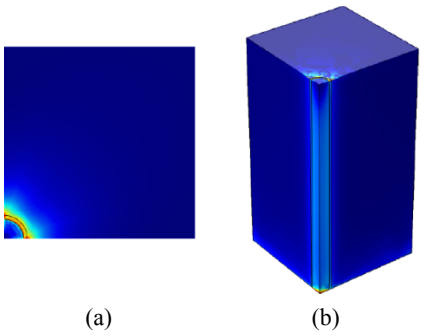
keep-out zone (KOZ) needs to be considered for thermal TSVs (TTSVs) application.

In this paper, an analytical heat transfer model with transverse and longitudinal thermal resistance for TTSVs is proposed. In TTSVs, thermal stress impact on carrier mobility in active areas based on physical heat transfer analysis and simulation results is considered. Compared with the published 1D model, thermal properties, obtained by varying geometrical parameter of the TSV and related materials, of the proposed analytical heat transfer model are much closer to the corresponding Finite Element Analysis (FEA) simulated results. Therefore, the proposed analytical heat transfer model is valuable for guiding thermal design of 3D integrated systems. And KOZ consideration improves the thermal-mechanical reliability of the whole thermal mitigation system. At last, a case study of a two-layer stacked power system containing TTSVs is given to verify the accuracy and efficiency of the analytical model.

II. Analytical Heat Transfer Model

The proposed structure of TTSVs-based two-layer stacked power system is shown in Fig. 1. Power cells are abstractions of real power devices. During the operation, devices generate heat behaving as heat sources and temperature also increases for Joule heating. So, a power cell can be set to a unit cell which is surrounded by four Cu-TSVs which act as auxiliary heat dissipation paths.

Firstly, the KOZ when TSVs are used to conduct heat is derived. The mobility change of carriers caused by thermal stresses of TTSV can be expressed by



(a) (b)

Fig. 2. (a) and (b) are top and cross section view of FEA model, respectively.

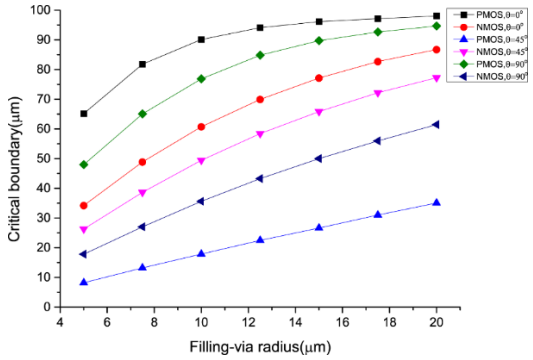


Fig. 3. Critical boundary for various filling-via radius.

$$\frac{\Delta\mu}{\mu}(r,\theta) = \pi \times \sigma_{rr} \times \beta(\theta) \tag{1}$$

where π is the piezoresistive coefficient, σ_{rr} is the TSV-induced radial stress and $\beta(\theta)$ is the orientation factor. The radial stress distribution can be obtained by FEA simulation and the simulation model is constructed as shown in Fig. 2. For reducing the computation time, only one quarter of the TSV structure is built due to the symmetry in axial directions. Based on the 5% carrier mobility change criterion and Eq. (1), the critical boundary of KOZ under 380K thermal load for TSVs with filling-via radius varies from 5 μm to 20 μm, and 1 μm dielectric layer thickness is plot in Fig. 3, where θ is the angle between transistor's channel and radial stress. As we can see, for PMOSFET, when θ is 0°(TSV-induced stress is parallel to PMOS channel), the critical boundary of KOZ has maximum value. As the radius of filling-via increases, the corresponding KOZ boundary goes up. The distance between the nearest two neighbor TSVs is big enough in the simulation model. Therefore, the effect of interaction between TSVs on the KOZ can be ignored.

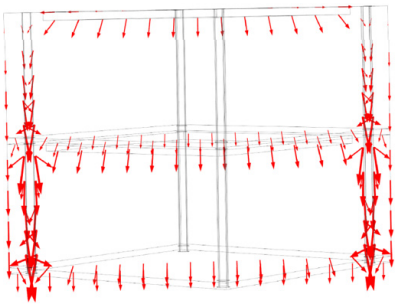


Fig. 4. Cross section view of detailed thermal flux in diagonal direction of the heat mitigation structure.

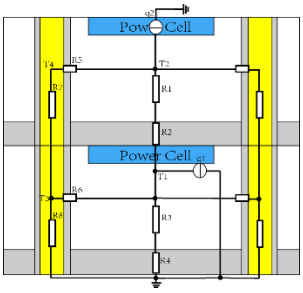


Fig. 5. Thermal resistance network model for heat mitigation structure corresponding to Fig. 4.

There are mainly two paths for heat flowing from the power cell to the ambient. The first one is from the power cell to the bulk silicon and then to the bonding layer. Another one is from the power cell to the TSV structure. Most of heat dissipate from the TSV owing to the high thermal conductivity of the Cu pillar and there is still some heat dissipating from Cu pillar to the bulk silicon. The comparability of heat transfer and current flow can be applied for thermal analysis in a simple or more complex system. From the analysis of thermal path in the previous case, a detailed thermal flow diagram which also has been verified by FEA simulation shown in Fig. 4 and a thermal resistance network shown in Fig. 5 can be derived, respectively.

As shown in the thermal resistance network, two heat sources are replaced by current sources q1 and q2. Similar to Kirchhoff's Circuit Law and Kirchhoff's Voltage Law in electronic circuits, we can derive

$$q_1 = \frac{T_1}{R_3+R_4} + \frac{T_1-T_3}{R_6} - \frac{T_2-T_1}{R_1+R_2} \tag{2}$$

$$q_2 = \frac{T_2-T_1}{R_1+R_2} + \frac{T_2-T_4}{R_5} \tag{3}$$

$$\frac{T_2-T_4}{R_5} = \frac{T_4-T_3}{R_7} \tag{4}$$

$$\frac{T_1-T_3}{R_6} + \frac{T_4-T_3}{R_7} = \frac{T_3}{R_8} \tag{5}$$

Rearrange equations from (2)-(5), yields

$$\left(\frac{1}{R_3+R_4} - \frac{1}{R_1+R_2} + \frac{1}{R_6}\right)T_1 - \frac{1}{R_1+R_2}T_2 - \frac{1}{R_6}T_3 = q_1 \tag{6}$$

$$-\frac{1}{R_1+R_2}T_1 + \left(\frac{1}{R_1+R_2} + \frac{1}{R_5}\right)T_2 - \frac{1}{R_5}T_4 = q_2 \tag{7}$$

$$\frac{1}{R_5}T_2 + \frac{1}{R_7}T_3 - \left(\frac{1}{R_5} + \frac{1}{R_7}\right)T_4 = 0 \tag{8}$$

$$\frac{1}{R_6} - \left(\frac{1}{R_6} + \frac{1}{R_7} + \frac{1}{R_8}\right)T_3 + \frac{1}{R_7}T_4 = 0 \tag{9}$$

Thermal resistance is proportional to the thermal path length and inverse proportional to the product of thermal conductivity of the material and area of the thermal path, which is

$$R = \frac{L}{\kappa \cdot S} \tag{10}$$

Then thermal resistance for each element is giving as follows:

$$R_1 = \frac{(b-a)/2}{\kappa_{Si}\left(\frac{a+b}{2}\right)^2} + \frac{H_1-(b-a)/2}{\kappa_{Si}\left(b^2-4\pi r^2\right)} \tag{11}$$

$$R_2 = \frac{tb_1}{\kappa_{SiO_2}\left(b^2-4\pi r^2\right)} \tag{12}$$

$$R_3 = \frac{(b-a)/2}{\kappa_{Si}\left(\frac{a+b}{2}\right)^2} + \frac{H_2-(b-a)/2}{\kappa_{Si}\left(b^2-4\pi r^2\right)} \tag{13}$$

$$R_4 = \frac{tb_2}{\kappa_{SiO_2}\left(b^2-4\pi r^2\right)} \tag{14}$$

$$R_5 = \frac{1}{4}\cdot 2\int_{r-\frac{d}{\cos\alpha}}^{r} \frac{dl}{\kappa_{SiO_2}\pi l\left(H_1+tb_1\right)} + \frac{\pi}{\kappa_{Cu}2\left(H_1+tb_1\right)} = \frac{-\ln\left(1-\frac{d}{r\cos\alpha}\right)}{2\pi\kappa_{SiO_2}\left(H_1+tb_1\right)} + \frac{\pi}{\kappa_{Cu}2\left(H_1+tb_1\right)} \tag{15}$$

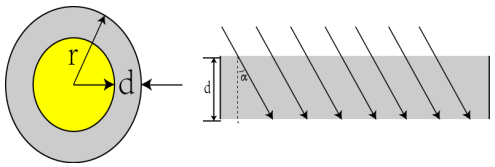


Fig. 6. Detailed schematic diagram of heat entering from bulk Si to TSV liner SiO_2.

$$R_6 = \frac{1}{4}\cdot 2\int_{r-\frac{d}{\cos\alpha}}^{r}\frac{dl}{\kappa_{SiO_2}\pi l\left(H_2+tb_2\right)}+\frac{\pi}{\kappa_{Cu}2\left(H_2+tb_2\right)} \tag{16}$$

$$=\frac{-\ln(1-\frac{d}{r\cos\alpha})}{2\pi\kappa_{SiO_2}\left(H_2+tb_2\right)}+\frac{\pi}{\kappa_{Cu}2\left(H_2+tb_2\right)}$$

$$R_7 = \frac{1}{4}\cdot\frac{H_1+tb_1}{\kappa_{Cu}\pi(r-d)^2} \tag{17}$$

$$R_8 = \frac{1}{4}\cdot\frac{H_2+tb_2}{\kappa_{Cu}\pi(r-d)^2} \tag{18}$$

First terms on the right side of Eqs. (11) and (13) result from small heat source enters in bigger conduction area and leads to thermal spreading resistance. To simplify the complicated analytical expressions for the spreading resistance, usually the thermal spreading angle is chosen 45°. In Eqs. (15)-(18), the coefficients 1/4 results from the fact that one power cell is surrounded by four TTSVs and these TTSVs are in parallel in equivalent thermal network shown in Fig. 5. The lower and upper limit of integral in Eqs. (15) and (16) is depicted in Fig. 6. First and second term of Eqs. (15) and (16) represents transverse resistance of TSV liner and TSV filling-via, respectively. Heat flows from Si to TSV liner with specific angle α which actually enlarge the thermal path of the TSV liner transverse resistance. Substitute Eqs. (11)-(18) into Eqs. (6)-(9), temperature rise for each layer can be derived.

Similar to Eqs. (2)-(18), the following relationships for 1D thermal resistance network shown in Fig. 7 can be derived, which are

$$\frac{-1}{R_{11}+R_{22}}\cdot T_1+\frac{1}{R_{11}+R_{22}}\cdot T_2 = q_2 \tag{19}$$

$$\frac{1}{R_{33}+R_{44}}\cdot T_1 = q_1+q_2 \tag{20}$$

where R_{11} and R_{33} are effective thermal resistance for the 1st and 2nd Si layer, and R_{22} and R_{44} are effective

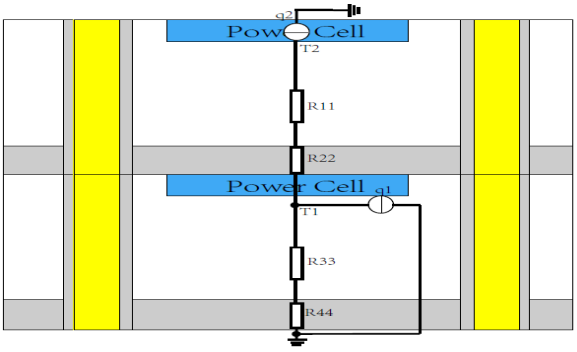


Fig. 7. 1D thermal resistance network.

thermal resistance for the 1st and 2nd bonding layer. Their detailed expressions can be derived using effective thermal conductivity for each layer containing TSV structures.

III. Simulating and Discussions

Material for the bonding layer and TSV liner is silicon oxide and the filling-via material is Cu. Thermal conductivity for silicon, silicon oxide and copper, namely σ_{Si}, σ_{SiO2}, σ_{Cu}, is 130 W/(m·K), 1.38 W/(m·K), 400 W/(m·K),respectively. Angel α is also assumed to be 45°.We assume the power cell is composed of PMOS device and the angle θ is 45°. From Fig. 3 we can find that the minimum KOZ boundary for filling-via radius range from 5 μm to 20 μm is 35.08 μm .The heat source power for each layer on the surface is 1W. The bottom surface adjacent to the heat sink is set 27 °C which assumes the heat exchange coefficient is approaching infinity for the heat sink. The rest of the surfaces are adiabatic. Fig. 8 to 11 shows the temperature difference with respect to the filling-via radius, thickness of bulk Si, TSV liner thickness and thickness of bonding layer, respectively. Meanwhile the proposed model is compared with the FEA simulation and the 1D model result to verify its accuracy.

As shown in Fig. 8, the temperature difference decreases as the filling-via radius increases due to the high thermal conductivity of Cu than the Si. Although 1D model describes the same tendency, it loses accuracy compared to the proposed model. As the filling-via radius goes up, the first terms on the right hand of Eqs. (15) and (16) decrease which means the thermal blockage effect of silicon oxide becomes weak but 1D model only considers the longitudinal resistance and 1D model overestimates

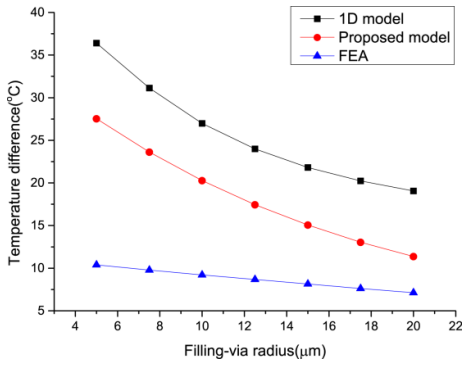


Fig. 8. Temperature difference with respect to filling-via radius of TSV. The other parameters are d=1 μm, tb1=tb2=10 μm, H1=H2=200 μm.

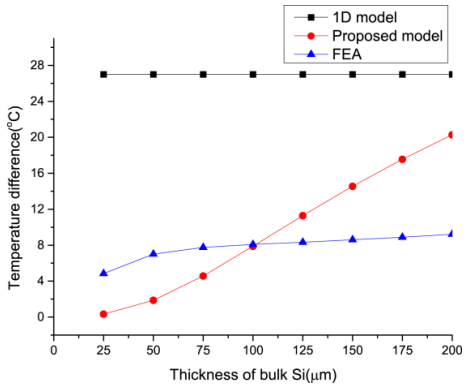


Fig. 9. Temperature difference with respect to thickness of bulk Si. The radius of filling-via is 10 μm and the other parameters are d=1 μm, tb1=tb2=10 μm.

the heat management design.

In Fig. 9, both FEA result and proposed model show the temperature difference increases when the thickness of bulk Si increases. However,1D model shows only a little decrease where the increase of effective thermal conductivity can compensate the increase of the thermal length.

In Fig. 10, the proposed model finally approaches the FEA result while the 1D model almost remains constant because the effective thermal conductivity keeps nearly unchanged due to the tiny change of liner thickness.

As illustrated in Fig. 11, bonding layer thickness has a significant impact on the temperature rise and acts more like a thermal barrier between Si layers. The temperature rise increases as the bonding layer thickness goes up. Both the 1D model and proposed model show the same relationship while 1D model shows larger error when the bonding layer thickness goes down and the typical bonding layer thickness in 3D integration process is 10 μm.

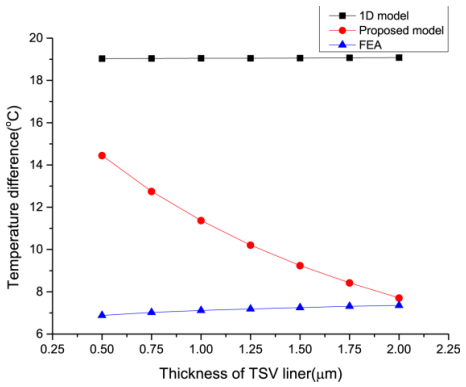


Fig. 10. Temperature difference with respect to TSV liner thickness. The radius of filling-via is 20 μm and the other parameters are tb1=tb2=10 μm, H1=H2=200 μm.

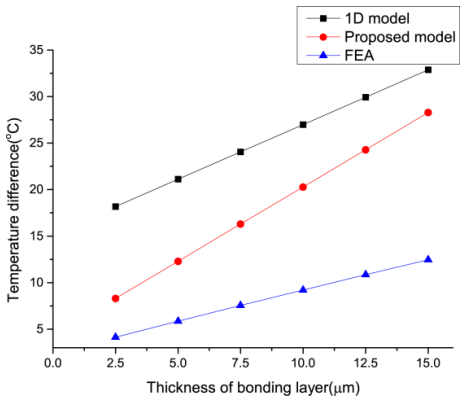


Fig. 11. Temperature difference with respect to thickness of bonding layer. The radius of filling-via is 10 μm and the other parameters are d=1 μm, H1=H2=200 μm.

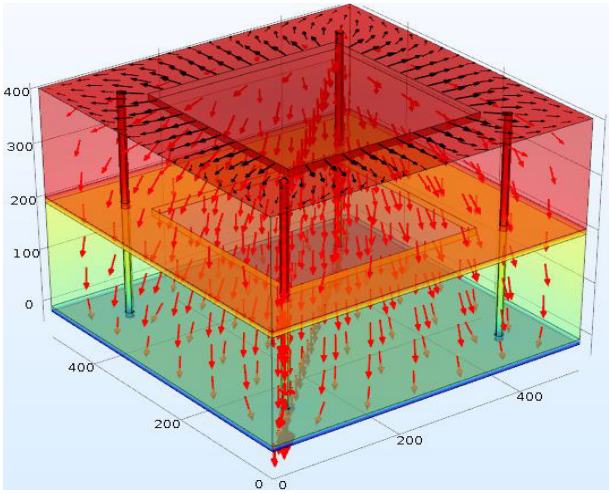


Fig. 12. FEA model based on COMSOL software.

Fig. 12 shows exact FEA model based on COMSOL software. The length and width are both set 500 μm, and each power cell consumes 1W of power which occupies

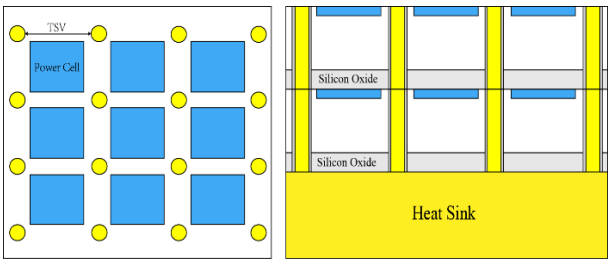


Fig. 13. 2-layers stacked power system using TTSVs as thermal mitigation tool.H1=H2=150 μm, tb1=tb2=10 μm, d=1 μm and the filling-via radius is 20 μm.

300 μm × 300 μm area. Other parameters such as filling-via radius, thickness of bulk Si, TSV liner thickness and thickness of bonding layer are variables, which can be changed in every FEA simulation.

IV. Case Study

The analytical model has been applied to a 3D stacked power system with internal TTSVs as a heat dissipation method. The construction of this 3D integrated system is shown in Fig. 13. The size for each power cell is 300 μm × 300 μm and generated power for each is 1W. The bottom surface of the heat sink made of copper is set constant temperature at 293.15K and the rest surfaces of the stacked structure are adiabatic which is close to the practical package case. The FEA simulation result shows that the steady state temperature of the top layer is 304.51K and for the bottom layer is 301.33K. The temperature rise is 3.18K between two layers due to the large filling-via radius and thinned bulk Si thickness. The analytical model gives 6.96K temperature rise and the 1D model has 10.17K temperature rise. Thus, the analytical model is superior than the 1D model in the proposed heat mitigation structure. Though FEA result is much more accurate but this method is extremely time consuming for chip scale numerical analysis. It takes less than 1 second for the analytical and 1D model, which is much shorter compared to the FEA method that consuming 7 minutes in a small computer workstation with 64GB memory.

V. Conclusions

In summary, we have proposed a heat mitigation structure based on the consideration of the impact of TTSV thermal stress on the carrier mobility changes. We have shown the relationship between temperature difference in two layers and the filling-via radius, thickness of bulk Si, thickness of TSV liner as well as bonding layer thickness using the proposed analytical model and the 1D model without any curve fitting coefficients which can be extended to more than two layers situations. Both the FEA results and the proposed analytical model are helpful in the heat management design of 3D ICs and its reliability improvement.

Acknowledgments

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References

[1] X. Xu, A. Karmarkar, 3d tcad modeling for stress management in through silicon via (tsv) stacks, AIP Conference Proceedings 1378 (1) (2011) 53–66.

[2] T. Jiang, C. Wu, L. Spinella, J. Im, N. Tamura, M. Kunz, H.-Y. Son, B. Gyu Kim, R. Huang, P. S. Ho, Plasticity mechanism for copper extrusion in through-silicon vias for three-dimensional interconnects, Applied Physics Letters 103 (21) (2013) 211906.

[3] H.-C. Cheng, T.-C. Huang, P.-W. Hwang, W.-H. Chen, Heat dissipation assessment of through silicon via (tsv)-based 3d ic packaging for cmos image sensing, Microelectronics Reliability 59 (2016) 84 – 94.

[4] D. Qiu, L. Cao, Q. Wang, F. Hou, X. Wang, Experimental and numerical study of 3d stacked dies under forced air cooling and water immersion cooling, Microelectronics Reliability 74 (2017) 34 – 43.

[5] P. M. Souare, V. Fiori, A. Farcy, F. de Crcy, H. B. Jamaa, A. Bor- bely, P. Coudrain, J. P. Colonna, S. Gallois-Garreignot, B. Gi- raud, S. Cheramy, C. Tavernier, J. Michailos, Thermal effects of silicon

thickness in 3-d ics: Measurements and simulations, IEEE Transactions on Components, Packaging and Manufacturing Technology 4 (8) (2014) 1284–1292.

[6] Y. Shin, S. E. Kim, S. Kim, Thermal assessment of copper through silicon via in 3d ic, Microelectronic Engineering 156 (2016) 2 – 5, mAM (Materials for Advanced Metallization) 2015.

[7] A. Jain, R. E. Jones, R. Chatterjee, S. Pozder, Z. Huang, Thermal modeling and design of 3d integrated circuits, in: 2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2008, pp. 1139–1145.

[8] J. L. Ayala, A. Sridhar, D. Cuesta, Thermal modeling and analysis of 3d multi-processor chips, Integration, the VLSI Journal 43 (4) (2010) 327 – 341.

[9] F. Wang, N. Yu, Thermal management of coaxial through- silicon-via (c-tsv)-based three-dimensional integrated circuit (3d ic), IEICE Electronics Express 13 (11) (2016) 20151117–20151117.

[10] Z. Liu, S. Swarup, S. X. D. Tan, Compact lateral thermal resistance modeling and characterization for tsv and tsv array, in: 2013 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2013, pp. 275–280.

[11] Z. Liu, S. Swarup, S. X. D. Tan, H. B. Chen, H. Wang, Compact lateral thermal resistance model of tsvs for fast finite-difference based thermal analysis of 3-d stacked ics, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 33 (10) (2014) 1490–1502.

[12] H. Xu, V. F. Pavlidis, G. D. Micheli, Analytical heat transfer model for thermal through-silicon vias, in: 2011 Design, Automation Test in Europe, 2011, pp. 1–6.

[13] B. Huang, Z. Wu, The thermal analysis study of 3d bare chip laminated packaging structure, AIP Conference Proceedings 1890 (1) (2017) 040054.

[14] S. K. Ryu, K. H. Lu, T. Jiang, J. H. Im, R. Huang, P. S. Ho, Effect of thermal stresses on carrier mobility and keep-out zone around through-silicon vias for 3-d integration, IEEE Transactions on Device and Materials Reliability 12 (2) (2012) 255–262.

[15] M. Y. Tsai, P. S. Huang, C. Y. Huang, H. Jao, B. Huang, B. Wu, Y. Y. Lin, W. Liao, J. Huang, L. Huang, S. Shih, J. P. Lin, Investigation on cu tsv-induced koz in silicon chips: Simulations and experiments, IEEE Transactions on Electron Devices 60 (7) (2013) 2331–2337.

[16] Y. Pi, W. Wang, Y. Jin, An accurate calculation method on thermal effectiveness of tsv and wire, in: 2016 IEEE 18th Electronics Packaging Technology Conference (EPTC), 2016, pp. 569–573.

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