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Neural Spike Detection Circuit with Amplification Method using Input DC Level Control

Jong Pal Kim

***Abstract*—A neural spike detection circuit is presented, in which all the amplifiers have an open loop architecture to reduce area and current consumption fundamentally. A new method for controlling the gain of an open loop amplifier is proposed. The gains of instrumentation amplifier (IA) and multiplier are controlled by a DC level of the input. In addition, an instrumentation amplifier (IA) includes a compensation circuit against the fabrication process corners to prevent amplification failure. The compensation circuit detects and adds threshold voltage variations in the compensation feedback loop. The circuit is fabricated using the standard 0.18 μm CMOS process. Changing the DC level at the IA input results in the amplification gain increase up to 650 V/V. The nonlinear amplification control capability of the multiplier is verified as the DC input level changes. The minimum detectable amplitude of neural spike is 100 μVpk. The overall power consumption is 1.4 μW. Integrated input-referred noise is measured to be 7.1 μVrms in a frequency range of 100 Hz to 10 kHz.**

***Index Terms*—Electroceuticals, implantable device, neural spike, IA, instrumentation amplifier**

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School of Mechatronics Engineering, Korea University of Technology and Education, 1600, Chungjeol-ro, Byeongcheon-myeon, Dongnam-gu, Cheonan-si, Chungcheongnam-do, 31253, Korea
E-mail : jongpalk@koreatech.ac.kr

I. INTRODUCTION

At the 2018 World Economic Forum, electroceuticals was selected as the next promising technology that can overcome the shortcomings of chemical drugs [1]. The transmission of information from body organs to the brain and control signals from the brain to body organs are based on digital electrical signals in the form of spikes through nerves. An electroceuticals is a compound word of electronic and pharmaceuticals, and is a device that electronically reads and manipulates electrical spike signals in nerve signals to produce the efficacy of drugs. Fig. 1 shows the configuration of connections between neurons and electroceuticals for manipulation of nerve signals. In open-loop electroceuticals, it usually consists only of a stimulator and a digital control unit. Since electronic medicine is inserted and used in the human body, reliability is very important factor. It is necessary to check whether the stimulation current is actually injected and the stimulation current threshold at which nerve signals are activated by the stimulus current. For this reason, a readout channel (*READOUT_CHANNEL*)

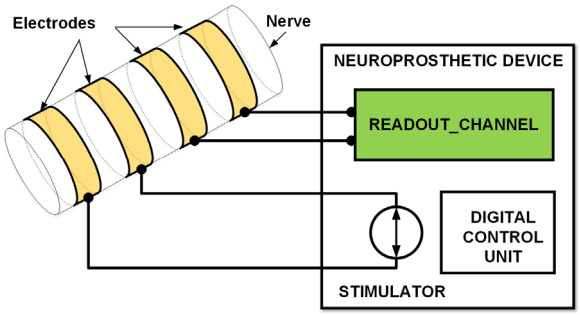

Fig. 1. Interface configuration between neuron and electroceuticals.

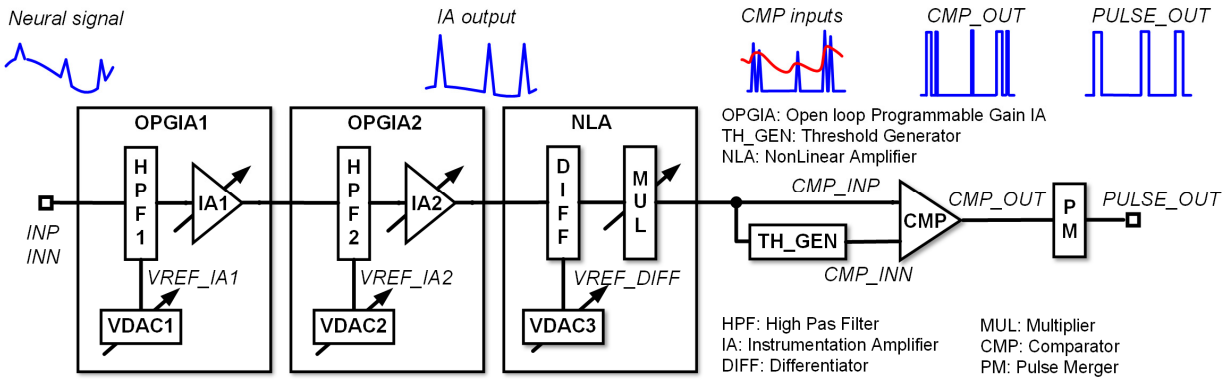

Fig. 2. Top view of readout channel.

in Fig. 1 is required even in open loop electroceuticals.

Implantable devices for electroceutical applications require very low power consumption and a small form factor. The readout channel used to amplify the neural signal must also have a low power consumption and a small area. Traditional amplifiers have a closed loop architecture that uses output feedback to the input. The widely used capacitively coupled IA (CCIA) is a representative example [2-5]. The CCIA has precise gain characteristics, but the input and feedback capacitors for gain and the Miller capacitor for stability occupy area. The open loop architecture amplifier does not require input/feedback capacitors for gain and does not use feedback, so no Miller capacitor for stabilization is required. If there is a way to adjust only the amplification gain, the open loop type amplifier has a fundamental advantage in terms of area. In the case of an open loop amplifier, the amplification gain distribution may be larger than that of a closed loop amplifier. However, in measuring the neural spike signal, the distribution of the amplification gain among chips is not important. This is because the absolute magnitude of the nerve spike signal does not matter. Neural information is delivered as the frequency of spikes per unit time. In a closed loop amplifier, the phase-shifted output signal in the high-frequency region can be fed back to the input and cause oscillation. For this reason, a large compensation cap is added to deliberately reduce the bandwidth. Because of this stability compensation, the bandwidth is lowered, and additional current consumption is required to secure the desired bandwidth. Therefore, the open loop amplifier fundamentally has a smaller area and lower current consumption compared to the closed loop amplifier.

In this work, an ultralow power neural amplifier circuit with on-chip spike detection is presented. For low power and low area, the open loop architecture is selected for amplifiers, and a method of controlling the input DC level is proposed as a means for adjusting the amplification gain. In the front-end stage, the gain of the open loop programmable gain IA (OPGIA) is controlled using the input DC level adjustment. Also, for the first time, the input DC level is used to adjust the amplification gain of a multiplier.

Section II shows the architecture of this work. Section III shows the circuit description. Section IV and V show the measurement results and conclusion.

II. ARCHITECTURE

A top configuration of the neural spike detection circuit is shown in Fig. 2. In order to reduce power consumption, ADC and digital processing method is replaced by a comparator-based approach for neural spike detection. Two IA (*IA1* and *IA2*) and nonlinear amplifier (*MUL*) are placed in series for sufficient gain. DC offset and low frequency fluctuation are eliminated by high pass filters (*HPF1* and *HPF2*) and differentiator (*DIFF*) before IAs and *MUL*, respectively. The reference voltages (*VREF_IA1* and *VREF_IA2*) of the high pass filters are also supplied to the DC inputs of IAs (*IA1* and *IA2*), respectively, and are used to adjust voltage gain of IAs. The DC output of the *DIFF* is generated by the voltage DAC (*VDAC3*) and is provided to the DC input of *MUL*, which can also regulate the amplification gain. The sufficiently amplified analog spike signal is

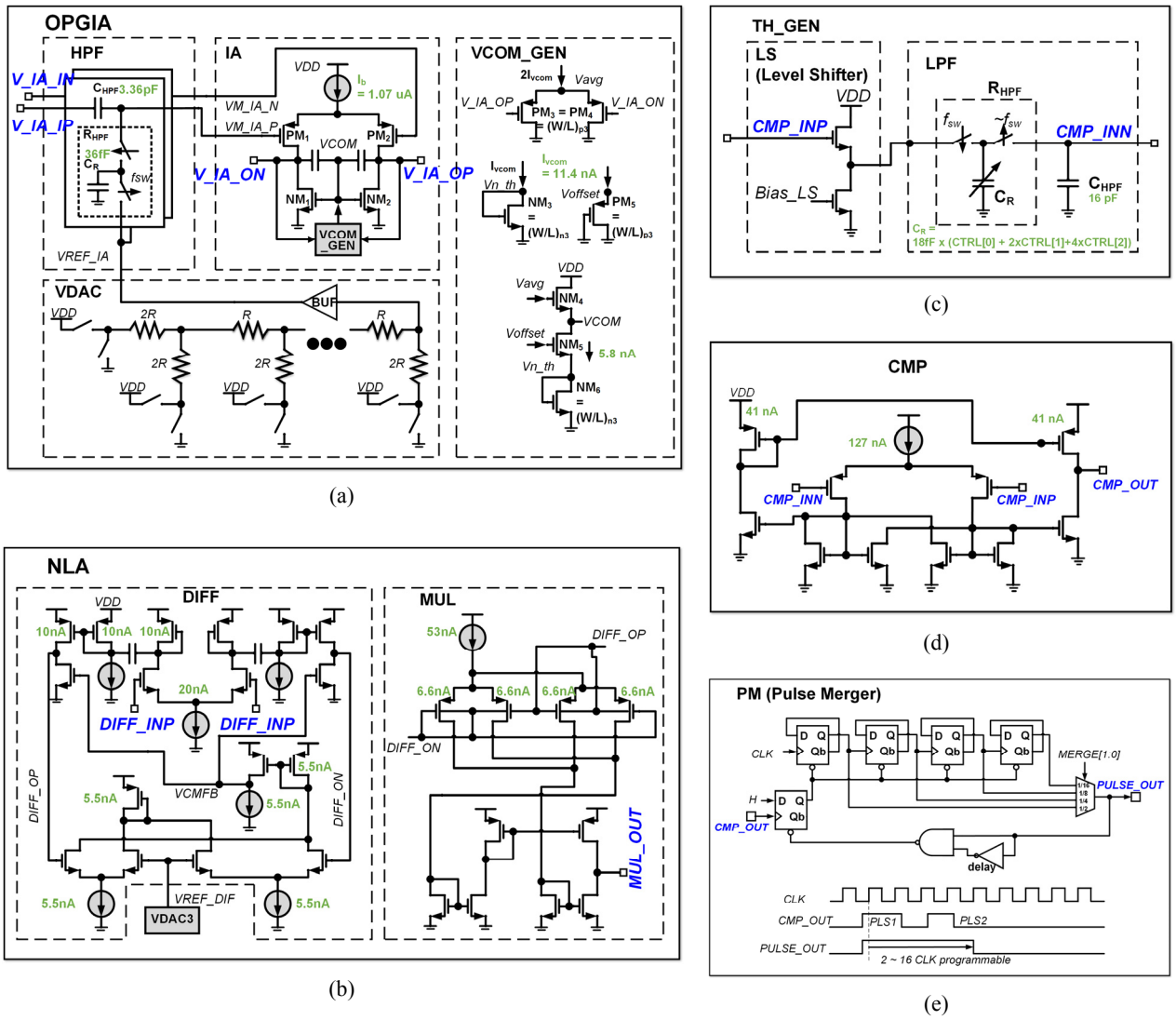

Fig. 3. Detail circuit structures of (a) open-loop programmable gain IA (OPGIA), (b) nonlinear amplifier (NLA), (c) threshold generator (TH_GEN), (d) comparator (CMP), (e) pulse merger (PM).

converted into a digital signal by a comparator (*CMP*). The comparison reference signal of the comparator is generated by the threshold generator (*TH_GEN*). Even if there is a single nerve spike, several adjacent pulses may appear at the output of the comparator due to a nonlinear process, and the output signal of the comparator is digital but the pulse width is not constant. Pulse merger (*PM*) combines neighboring pulses that cannot be physiologically continuously generated for a short time into one pulse, and makes the pulse width constant. All analog circuits are designed with a supply voltage of 0.6 V.

III. Circuit Description

In order to use a low operating voltage of 0.6 V, the circuit is designed using a moderate threshold device instead of a normal threshold device. The threshold voltages for the moderate threshold PMOS and NMOS are 140 mV and 270 mV, respectively.

Fig. 3 shows the detailed circuit for amplification and filtering. The amplification gains of both *OPGIA* and *NLA* are controlled by the input DC level.

Fig. 3(a) shows the detailed circuit of *OPGIA*. At *IA*, the transconductance of the input MOS (*PM1* and *PM2*) is changed by the input DC value (*VREF_IA*), and the ac biosignal filtered by the high pass filter (*HPF*) is

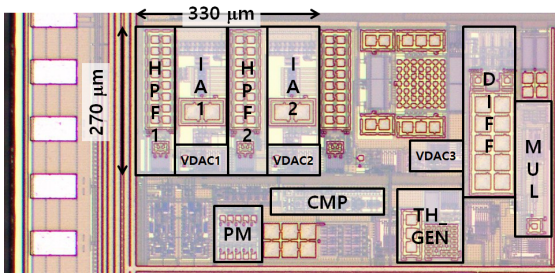

Fig. 4. Photograph of fabricated READOUT_CHANNEL.

amplified by the transconductance. The high pass filters consist of a capacitor (C_{HPF}) and a switched capacitor-based resistor (R_{HPF}). The equivalent resistance (R_{HPF}) for HPF can be freely adjusted with the switching frequency (f_{sw}). When a switching frequency of 100 kHz is applied, the high pass filter has a cutoff frequency of 150 Hz and the equivalent resistance value is 316 MΩ.

IA has a simple structure without no resistor or capacitor array for gain control. The gain of the IA is controlled by DC level at the input (*VM_IA_P* and *VM_IA_P*). The DC voltage at inputs of IA (*VM_IA_P* and *VM_IA_P*) is equal to the reference voltage (*VREF_IA*) supplied to the *HPF*. The DC level for IA gain control is generated by the voltage DAC(*VDAC*) with 6 bit resolution. In addition, for *IA*, a common voltage generator circuit (*VCOM_GEN*) is added to prevent amplification failure in some fabrication process corner conditions. The change in threshold voltage of the NMOS (NM_1/NM_2) according to the fabrication process variation is detected and compensated to the common mode feedback voltage (*VCOM*). The detailed circuit of *VCOM_GEN* is depicted in Fig. 3(a).

Fig. 3(b) shows the detailed circuit of *NLA*. The multiplier gain is also controlled by the input DC level as in *OPGIA*. The detailed structures of *DIFF* and *MUL* are depicted in Fig. 3(b) [6]. The output DC level of the differentiator is adjusted using voltage DAC (*VDAC3*) to obtain the required DC level of the multiplier input. The voltage of *VDAC3* is applied to the reference signal node (*VREF_DIFF*) in the common mode signal feedback circuit of the differentiator. The multiplier has a scheme of the gate-bulk input and operates as a nonlinear amplifier.

The threshold generator (*TH_GEN*) generates a threshold voltage for the comparator (*CMP*) input. TH_GEN takes the output of the *NLA* as an input and

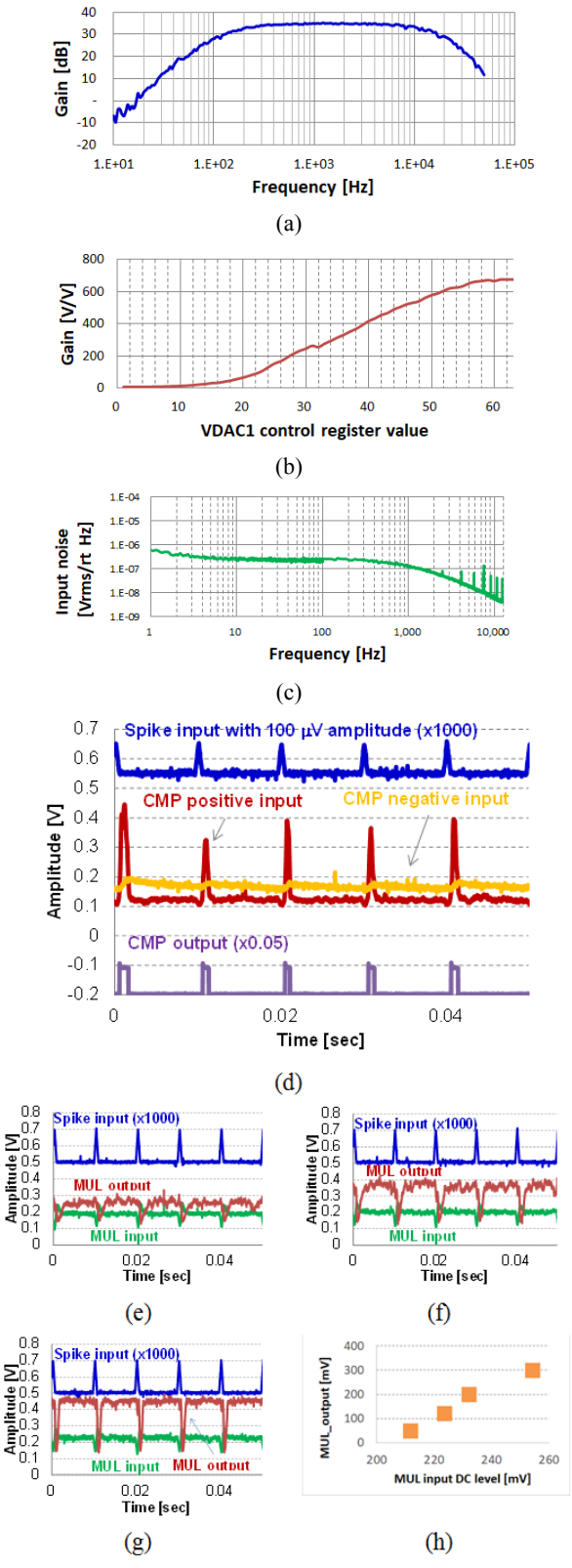

Fig. 5. Measurement results (a) frequency response example of IA, (b) gain of IA according to input DC level control, (c) input referred noise, (d) spike detection example with 100 μV input spike, (e)-(h) outputs of MUL according to the MUL input DC levels.

Table 1. Performance summary (measurements)

	This work	TBCAS'17 [7]	TBCAS'17 [8]	TBCAS'19 [9]
Fabrication process [um]	0.18	0.35	0.13	0.18
Supply voltage [V]	0.6	3	1.2	0.5
High pass freq. [Hz]	195	74~750	15~232	1
Low pass freq. [kHz]	11	6.34~9.4	5.2~10.2	6.8
Bandwidth, BW [kHz]	11	9.4	7.4	6.8
Amplifier architecture	**Open loop**	**Closed loop CCIA**	**Closed loop CCIA**	**Closed loop CCIA**
Gain control means	**Input DC**	**Cap. ratio**	**Cap. ratio**	**Cap. ratio**
Input cap./feedback cap. [F]	None	7.5p/100f	30p/125f	20p/200f
Current consumption, Ic [uA]	2.3	17.0	2.5	1.8
Readout channel area, A [mm^2]	0.20	0.17	0.21	0.16
Ic × A @BW=10kHz	**0.43**	**3.07**	**0.72**	**0.41**
Spike detection domain	Analog	Digital	Digital	Analog

CCIA: Capacitively Coupled IA

outputs a signal to be used as a comparison threshold through a level shifter and a low pass filter as shown in Fig. 3(c).

As shown in Fig. 3(d), the comparator used a generally well-known architecture. The comparator output can often output multiple adjacent pulses for one nerve spike input, which is due to noise and nonlinear operation through *DIFF* and *MUL*. Adjacent multiple pulses that cause neural spike count error are not simply removed by a hysteresis comparator. Therefore, an adjacent pulse merging circuit (*PM*) is designed, which merges the adjacent pulses within a predefined time window as shown in Fig. 3(e).

IV. MEASUREMENT RESULTS

The neural spike detection circuit is fabricated using the standard 0.18 μm CMOS process. The main blocks shown in Fig. 2 are marked on the die photo of Fig. 4. The measured transfer function example is shown in Fig. 5(a). The high-pass cut-off and low-pass cut-off frequencies of the transfer function are 195 Hz and 11 kHz, respectively. Fig. 5(b) shows the measured programmable voltage gain of the cascaded *OPGIA* in accordance with the voltage DAC (*VDAC1*) register control. Using the voltage DAC control will change the input DC level of the *IA* linearly, and the voltage gain of the *IA* reaches a maximum gain of 676 V/V. Fig. 5(c) shows the measured noise spectrum and the integrated input-referred noise is calculated to be 7.1 μVrms in a frequency range of 100 Hz to 10 kHz.

Fig. 5(d) shows the spike detection results with an input spike amplitude of 100 μV and intervals of 100 Hz. The positive and negative inputs of the *CMP* come from the outputs of *MUL* and *TH_GEN*, respectively. As mentioned in the previous section, the gain of the multiplier can be adjusted by the input DC level. Fig. 5(e)-(g) show the increased multiplier's outputs according to the increased multiplier's inputs. The correlation between the input DC level and the output peak amplitude of the MUL is summarized in Fig. 5(h). Supply voltage is 0.6 V, and current consumption of *IA*s, *DIFF*, *MUL*, and *CMP* is 2 μA, 60 nA, 100 nA, and 210 nA, respectively. The overall power consumption is 1.4 μW. Integrated input-referred noise is measured to be 7.1 μVrms in a frequency range of 100 Hz to 10 kHz. The measured performance is summarized in Table 1. This work was compared with previous works including CCIA and on-chip spike detection. All the previous works are equipped with closed loop CCIA type amplifiers, and the amplification gain is controlled by adjusting the ratio of the input and feedback capacitors [7-9]. To account for area and current consumption at the same time, a single new index is created by multiplying area and current consumption at the same bandwidth level, the lower the better. In the case of spike detection in the digital domain, it has an index value that is improved compared to previous works, and has a comparable level of the state-of-the-art work in the analog domain.

V. CONCLUSIONS

This paper presents a neural spike detection circuit, in which all the amplifiers have an open loop architecture to reduce area and current consumption fundamentally. A new method for controlling the gain of an open loop amplifier is proposed. The gains of the *OPGIA* and multiplier are controlled by a DC input. In addition, the *IA* incorporates threshold voltage detection and common mode feedback compensation circuit that can cope with changes in fabrication process conditions to prevent amplification failure. The circuit is fabricated using the standard 0.18 μm CMOS process. Changing the DC level at the IA input has shown that the amplification gain of the IA varies linearly up to 650 V/V. Amplification gain increase of the multiplier has been observed as the DC input level increases. It also showed that the spike detection circuit works well with an amplitude input of 100 μVpk.

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Jong Pal Kim received his B.S. degree in mechanical design from the Department of Mechanical Design, Chung-Ang University, Seoul, Korea, M.S. degree in mechanical engineering from KAIST, Daejon, Korea, and Ph.D. degrees in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 1995, 1997, and 2003, respectively. He was a member of research staff at Samsung Advanced Institute of Technology (SAIT) from 2001 to 2019. He was with IMEC at Belgium as a visiting researcher from 2010 to 2012. In 2020, he joined the Faculty of School of Mechatronics Engineering, Korea University of Technology and Education, Cheonan, Korea. His research interests include low power and low noise analog integrated circuits for biomedical and MEMS applications.