

High-speed Clock and Data Recovery System with Segmented Slew-rate Control Circuit for High-linearity in 65 nm CMOS Process

Kyunghwan Min, Sanggeun Lee, and Taehyoun Oh*

Abstract—A phase interpolator (PI) based all-digital clock and data recovery (CDR) system has been fabricated in 65 nm CMOS process. The segmented switching units control the slew rate of input clock signal in the PI and the linearity of PI control code and output phase shift steps is improved by 0.4 LSB for standard deviation of differential nonlinearity (DNL). The measurement results show that our CDR locks successfully for 6 Gbit/s non-return to zero (NRZ) high-speed signal with $2^{31}-1$ pseudo-random bit sequence (PRBS) pattern. The input NRZ input signal has 2.05 ps of root-mean square (RMS) jitter and 1 V_{dpp} of swing. When the loop is locked, the output clock signal shows 12.2 ps of peak-to-peak jitter and 1.826 ps of RMS jitter, which is divide 16 speed of the full rate. The measured phase noise of the recovered clock is -114.72 dBc/Hz at 1 MHz offset. The designed built-in pattern checker in receiver exhibits 10^{-12} of bit error rate (BER) at the center of data eye. The lock time of the loop measured via 7-bit monitoring digital-to-analog converter (DAC) is 54.5 ns. The prototype CDR occupies 0.073 mm² chip area and consumes 17.4 mW from 1.0 V power supply.

Index Terms—CDR, CMOS, data rate, HDMI, high-speed, integrated circuit, IO, loop, majority vote

I. INTRODUCTION

From requirement of high per-pin data speed between chip-to-chip communications, CDR circuits generate an optimized clock timing aligned to incoming random data with a small unit interval (UI). A CDR loop has been traditionally designed using charge pump-based loop filters along with analog voltage-controlled oscillators (VCO) [1-3]. Without careful design on the supply node, the control voltage can be coupled to the supply and it can be modulated to phase noise at the VCO output. In the digital-friendly circuits, the process-voltage-temperature variation and the effect of supply noise can be mitigated, and portability to a newer process can be improved as well [4]. The digital CDRs shown in [5-7] that operate with digital loop filters (DLF) have a good portability. IO schemes for many applications, such as DP, HDMI, PCI express, should support multi-channel timing recovery in receivers where frequency offsets between channels are zero. Implementing multiple PIs for each channel and sharing one oscillator can allow to achieve efficient power and area performances [8, 9]. PI-based CDRs should be able to catch up instantaneous frequency offsets between incoming data and recovered clock for resilient timing alignment for each channel. The integral path gain of each CDR with a bang-bang phase detector (PD) decides the frequency catch-up speed [10]. In this paper, we propose a 6 Gbit/s PI-based all-digital CDR that can support multi-channel implementation for HDMI 2.0 standard. The suggested majority voting logics update the digital loop filter without wasting deserialized edge information and the smooth movement

Manuscript received Feb. 23, 2021; reviewed May 24, 2021;
accepted May 27, 2021

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of PI control signal can be achieved. As a result, a low jitter performance has been measured when the loop locks. Due to the usage of two's complement format for the voted data, the counter blocks that only accumulates the vote can be obviated. Binary shifting gain extender at the end of the integration accumulators allows us to reduce the size of adders and to achieve a wide gain control range, while the previous scheme accumulates the data using counter [11, 12]. In the circuit's perspective, we have made a new slew rate control approach for PI to improve the DNL of the output clock phases. The better linearity between input digital control of the PI and output phase shifting steps contributes a stable loop gain. A Gray mapping can remove the abrupt transition of the codes.

The rest of the paper is organized as follows. Section II reviews the overall architecture of the proposed PI-based digital CDR. Section III presents the majority voting logics used for deserialized data. The section shows our DLF scheme, gain range extending structure, circuit diagram of our PI and the slew rate control scheme as well. Section IV shows the measurement results of our IP and Section V concludes this paper.

II. ARCHITECTURE

Fig. 1(a) presents the proposed 6 Gbit/s majority voting-assisted CDR architecture. As shown in Fig. 1(b), three half-rate strong-arm latches triggered by 3 GHz clocks at 0° , 180° and 90° timing, sample 3 Gbit/s ODD, EVEN, EDGE data, respectively. The early/late info is updated from the EDGE data when there is a transition in the $DATA_{IN}$ signal. In that case, either ODD or EVEN data is sampled as data 1 and thus the XOR gating of these two signals is one. 3:24 de-serializers transform 3×3 Gbit/s data into 24×375 Mbit/s parallel data and mitigate the power consumption and timing aligning difficulty from high-speed operation. The low-speed parallel CDR logics generate 8 EARLY and 8 LATE data from the previously sampled and deserialized ODD, EVEN, EDGE data. Integration of EARLY [7:0] and LATE [7:0] without losing EARLY/LATE info, requires 8 independent DLFs which increase power and chip area considerably. The majority voter reduces the parallel early/late data into 1-bit early/late data and thus the effect of parallel early/late data from parallel CDR logics can

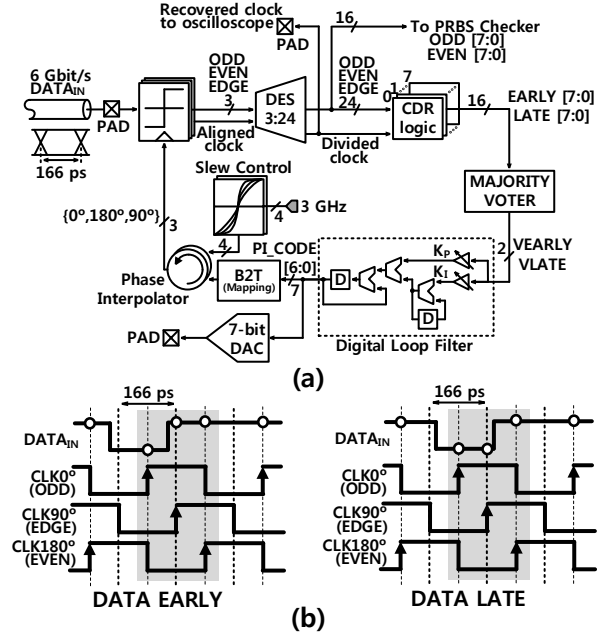


Fig. 1. (a) Architecture of the proposed PI-based CDR, (b) Illustration of the waveforms for 3 half-rate sampler latches at the front-end.

be statistically reflected on the 1-bit early/late signal [11, 12]. In the DLF, the programmable gain K_p and K_i control the closed loop bandwidth and jitter tolerance of CDR. The 5 LSB (least significant bit) bits out of 7-bit binary DLF outputs are encoded as a thermometer format in the binary-to-thermometer (B2T) block. The phase interpolators rotate the recovered clock phases from 0° to 360° for an optimal timing alignment. In front of the PI, the slew rate of clock signals coming from the oscillator is controlled by slew control blocks and the linearity of phase shifting steps is improved significantly. For a real-time measurement purpose, the 7-bit DAC monitors the DLF output in the analog data format. The PRBS checker with a BER calculator confirms if the received data accord with the transmitted data.

III. CIRCUIT DESCRIPTION

1. Voting Logics

Fig. 2(a) shows a logic circuit to decide the updating sign and Fig. 2(b) shows the majority voting logics. The EARLY [n] and LATE [n] signals are transformed to the voting number (+1:UP / 0:HOLD / -1:DOWN) by using Sign[n] and Mag[n] signals, where n is the integer

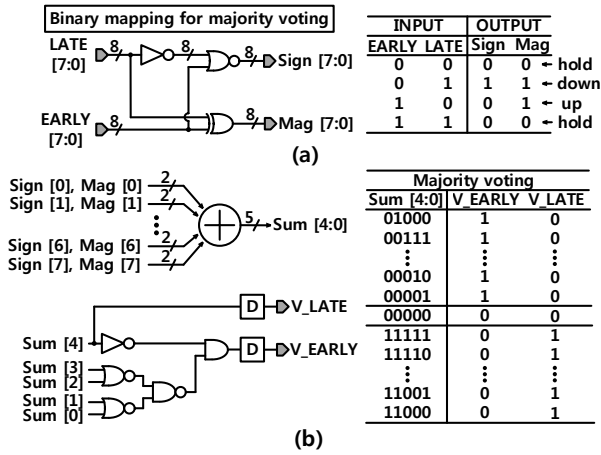


Fig. 2. Majority voting logic (a) binary mapping, (b) logic diagram.

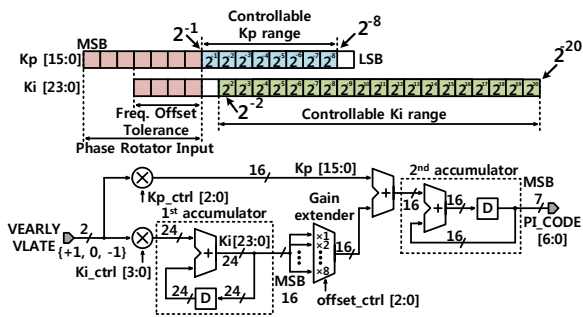


Fig. 3. Digital loop filter (DLF) circuit diagram and illustration of gain control procedure.

number from 0 to 7. When both EARLY [n] and LATE [n] are identical in which case clock signal and data signal are aligned, the output Sign [n] Mag [n] = 00 and no vote is contributed on Sum [4:0] signal. In the majority voting logics, the 8-bit voting numbers (+1 / 0 / -1) are summed up and the result spans the range from +8 to -8, which requires the Sum signal to have 5-bit two’s complement representation. +1 ~ +8 / 0 / -1 ~ -8 finally make the VEARLY, VLATE to be [10], [00], [01], respectively. When the CDR loop locks and Sum [4:0] stay on [00000], no update is made on the input of the following DLF. The EARLY [7:0] and LATE [7:0] signals are the recovered deserialized data [15:0] in our half-rate scheme. The built-in PRBS checker can measure BER to the range of $2^{-40} \approx 10^{-12}$ level [13].

2. Digital Loop Filter Scheme

Fig. 3 presents our DLF circuit schematic. VEARLY and VLATE bits mapped in two’s complement form are

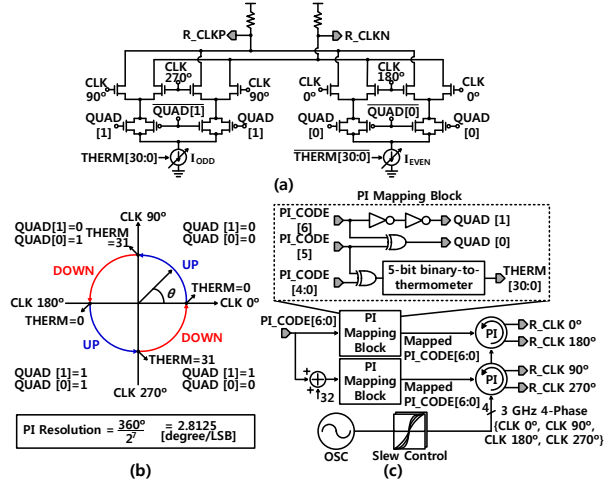


Fig. 4. (a) Circuit schematic of 7-bit phase interpolator, (b) Quadrature mapping of phase interpolator, (c) Description of a scheme for 2 phase interpolators for 0°, 180° and 90° clock timing recovery.

scaled by proportional gain (K_p) and integral gain (K_i) and the values are controlled via binary shifting as shown in Fig. 3. Expanding gain range of K_p and K_i has advantages of wide catch-up speed options for both phase offset and frequency offset in presence of a non-linear bang-bang PD [14]. Increasing K_i gain enables the loop to catch large frequency offset but concurrently widens the closed loop bandwidth of CDR and input jitter suppression effect is mitigated. The gain extender located in a proper position along the path does additional binary-shifting to increase the K_i range without concentrating large sized adders on the 1st accumulator only. If data and recovered clock have a frequency offset, the gain shifting degree in the gain extender controls follow-up speed as well. In a low frequency offset and large jitter environment at the input, the loop bandwidth is reduced by decreasing K_i gain. As like the scheme shown in [15, 16], a control signal of the PI (PI_CODE [6:0]) is monitored via the 7-bit DAC and the control patterns are sent out to the measurement equipment through an on-chip pad in the analog format.

3. Phase Interpolator and Slew Rate Control

Fig. 4(a) shows the circuit schematic diagram of our 7-bit PI that recovers the required timing by manipulating quadrature input clocks from 3 GHz oscillator. A current-steering PI can provide a highly linear phase shift [17, 18]. The resolution of phase interpolators depends on the

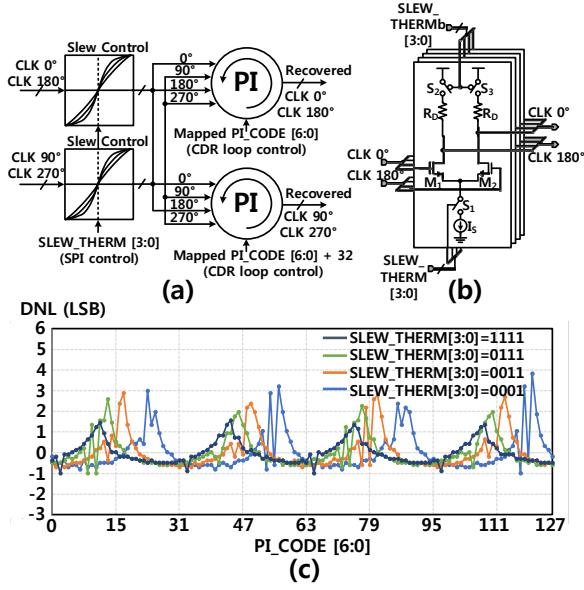


Fig. 5. (a) Circuit description of 2 slew rate control blocks and CLK 0°/180° PI, CLK 90°/270° PI, (b) Schematic for slew rate control, (c) DNL simulation results of phase shifting linearity.

binary bit number of PI_CODE [6:0] and increasing bit number aggravates the circuit complexity. As shown in the illustration of Fig. 4(b) our PI shows the resolution of 2.8 degree/LSB. To reduce a glitch, QUAD [1:0] are generated from 2 MSB bits of PI_CODE [6:0] using Gray-mapping. The rest PI_CODE [4:0], the binary LSB codes, are transformed to a thermometer code THERM [30:0] for fine DAC switching (I_{ODD} , I_{EVEN}). Fig. 4(c) shows a block diagram of overall PI circuits for half-rate CDR. 3 GHz quadrature clock signals are generated and provided from an oscillator for phase interpolation. The slew control blocks improve the linearity by increasing the slew rate, but the power performance should be traded-off. The half-rate CDR uses both CLK 0° / CLK 180° and CLK 90° for ODD/EVEN data sampling and EDGE data sampling, respectively. Since one PI can generate only two clock phases - 0°/180° or 90°/270°, two PIs are required to operate concurrently to all the required recovered clocks (0°, 180°, 90°). For initial CDR lock, CLK 0° and CLK 90° move simultaneously and 90° phase difference between 0°/180° and 90°/270° is maintained by adding 32 to the PI mapping block in the front.

Fig. 5(a) presents an architecture description of 2 slew rate control blocks for CLK 0°/180° PI, CLK 90°/270° PI. For slew rate control blocks to have equivalent loadings/timing delays, the clock signal CLK

0°/90°/180° /270° drive equally distributed gate loadings at PI inputs. The PI control code and shifted phase at the PI output have a non-linear relation due to the non-linear characteristics of devices and signals. Maintaining a good linearity for all range of control code results in a constant loop gain and stabilizes the loop transfer function. As shown in Fig. 5(b), 2-bit slew rate control blocks have been designed and placed at the input of PI block. The slew rate is controlled by turning on and off the segment unit. When the segmented block is disabled, the current mirror is switched off by S₁ and the loadings by S₂ and S₃. As the number of enabled block increases, g_m grows. Thus, the output clock signal makes a transition sharply. The graph on Fig. 5(b) shows the simulation results of the mapped PI_CODE [6:0] versus shifted output phase DNL in LSB unit for various slew options. Where N ranges from 0 to 127. As SLEW_THERM [3:0] increases from 0001 to 1111, the standard deviations of the DNLs are improved as 0.95, 0.86, 0.75 and 0.54 LSB. Using a fast slew for incoming quadrature clocks improves the linearity. However, the power increases as the number of enabled blocks increases. In our CDR, each segment unit consumes 0.285 mW. To achieve 0.86 DNL performance and 0.6 mW concurrently, we enable 2 segment units in the slew rate control blocks. Since the input of the block, SLEW_THERM [3:0], is thermometer coded. We enable 2 units out of 4 units.

IV. MEASUREMENT RESULTS

Fig. 1(a) shows the measurement nodes of our proposed CDR. To test our CDR, 6 Gbit/s 2^{31} -1 PRBS NRZ signal with 2.05 ps RMS jitter and 1 V_{dpp} swing at the input is generated by Synthesis Research BERT 7500B, as shown in Fig. 6(a). Fig. 6(b) presents the recovered clock jitter when the loop is locked and Tektronix TDS 6154C oscilloscope is used for measurement. The measured peak-to-peak and RMS jitter of the recovered clock (divided by 16) are 12.2 ps and 1.826 ps, respectively. The phase noise of recovered clock is measured by HP E4401B and is measured as -114.72 dBc/Hz at 1 MHz, as shown in Fig. 6(c). The lock pattern of the digital control of PI input is measured via a 7-bit DAC output via a signal from on-chip pad when the loop is initially turned on and finds the lock position, as

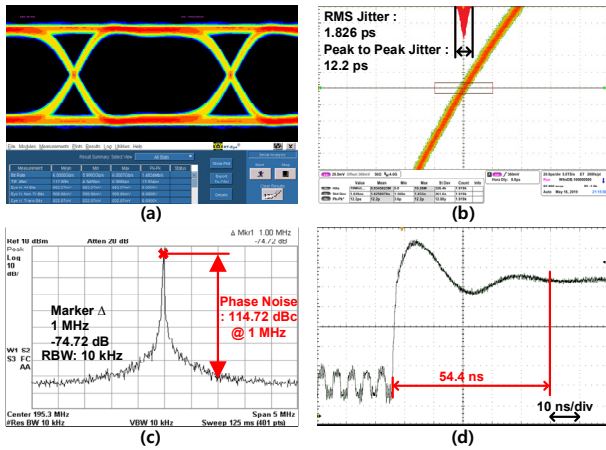


Fig. 6. (a) 6 Gbit/s input NRZ signal used for the measurement, (b) Recovered output clock jitter during steady state, (c) Measured output phase noise of the recovered clock, (d) Measured lock time of the CDR loop.

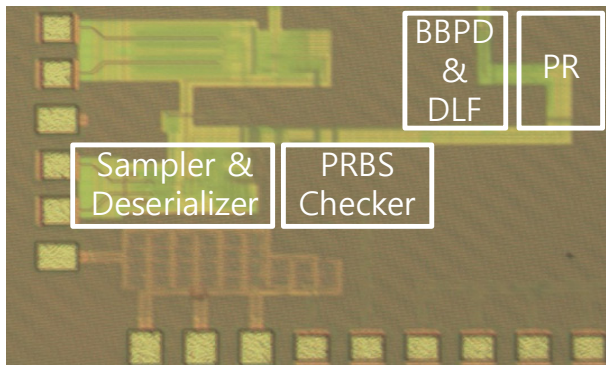


Fig. 7. Die photograph of the proposed CDR.

shown in Fig. 6(d). The measured lock time of the loop is 54.5 ns. The built-in PRBS checker shows the BER of under 10^{-12} at 6 Gbit/s at the centre of data eye. Fig. 7 shows the die photograph of the proposed PI-based all digital CDR. The prototype has been fabricated in 65 nm CMOS process and occupies 0.073 mm² chip area (excluding PRBS checker). In Table 1, the measurement results of the proposed CDR are summarized and compared to the prior arts. [3] presents a CDR scheme charge pump-based loop filter and it uses an analog $V_{control}$. The chip area is comparably large to reduce the ripple on the control voltage. [6, 8] have shown digital-type CDRs with digital loop filters and [8] generates the clock source from an analog charge pump PLL with a ring VCO. Our CDR is a digital filter-based and aligns the linearized PI output phase to data timing with a low jitter performance by an assistance from majority voting logics. The proposed CDR shows 17.4 mW of power

Table 1. Performance comparison table

	[3]	[6]	[8]	This work
Technology	65 nm CMOS	130 nm CMOS	180 nm CMOS	65 nm CMOS
Architecture	Analog filter-based CDR	Digital filter-based CDR	Digital filter-based CDR	Digital filter-based CDR
Supply (V)	1.0	1.2	1.4	1.0
Data rate (Gbit/s)	0.75–3.0	1.0–4.0	0.2–4.0	6.0
Peak-to-peak Jitter (ps)	37.2 (@ 3.0 Gbit/s)	29.2 (@ 3.0 Gbit/s)	115.1 (@ 2.0 Gbit/s)	12.2 (@ 6 Gbit/s)
RMS Jitter (ps)	5.69 (@ 3.0 Gbit/s)	3.58 (@ 3.0 Gbit/s)	28 (@ 2.0 Gbit/s)	1.83 (@ 6 Gbit/s)
BER	$< 10^{-12}$	$< 10^{-14}$	$< 10^{-12}$	$< 10^{-12}$
Power (mW)	15.5	11.4	14	17.4
FoM (mW/Gbit/s)	5.1	3.8	7	2.9
Area (mm ²)	0.35	0.074	0.8	0.073

consumption at 6 Gbit/s and the best jitter performances among the results of compared papers.

V. CONCLUSION

A half-rate PI-based all-digital CDR has been proposed. The segmented slew rate scheme improves the linearity of the phase steps. The proposed CDR is designed with all digital scheme and can be ported to other processes with reduced manpower. Our CDR consumes 17.4 mW power from 1.0 V supply at 6 Gbit/s. The prototype CDR occupies 0.073 mm² chip area and has been fabricated in 65 nm CMOS process.

ACKNOWLEDGMENTS

The work reported in this paper was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (NRF-2020R1F1A1057497) and present research has been conducted by the Excellent researcher support project of Kwangwoon University in 2021. The EDA Tool was supported by the IC Design Education Center.

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