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Effects of Pillar Conditions on DC/AC Characteristics of Tunnel Field-effect Transistor with Vertical Structures

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***Abstract*—To investigate the effects of various pillar conditions such as pillar thickness (T_{pillar}), pillar height (T_{Si}), and doping concentration of pillar on DC characteristics of TFETs with vertical structures ($TFET_{VS}$) and AC switching characteristics of $TFET_{VS}$ inverters, Mixed-mode device and circuit TCAD simulations are performed. As 1) the T_{pillar} is thicker, 2) the T_{Si} is increased, and 3) the doping concentration of the pillar is reduced, the tunneling current between source and channel gets increased and the gate-to-drain capacitance (C_{GD})-gate voltage (V_G) curve becomes positive-shifted due to the weaker controllability of V_G on the drain-side channel. Through the transient responses of $TFET_{VS}$ inverters with various pillar conditions, it is revealed that AC switching performance can be improved by the enhanced tunneling current and the positive-shifted C_{GD}-V_G curve caused by the weaker V_G controllability on the drain-side channel.**

***Index Terms*—TFET, vertical structure TFET, AC switching characteristics of TFET**

I. INTRODUCTION

For the low power consumption of metal–oxide–semiconductor field-effect transistors (MOSFETs), supply voltage (V_{DD}) needs to be scaled down. Furthermore, for maintaining high on-current (I_{ON}) despite of the V_{DD} reduction, extremely low subthreshold swing (*SS*) is necessary. However, it is well-known that the *SS* of a MOSFET cannot be lowered below 60 mV/dec at room temperature because its operation is based on thermionic carrier injection [1]. A tunneling field-effect transistor (TFET) has been regarded as one of the most promising candidates for a next-generation low-power device due to its low *SS* (sub-*kT/q SS* at room temperature) and excellent complementary MOS (CMOS) process compatibility [2-4]. However, there are still a lot of challenges in the way to commercialization: particularly, ambipolar current by undesirable drain-side tunneling and low I_{ON}.

In order to overcome these disadvantages, TFETs with elevated drain ($TFET_{ED}$) have been proposed since $TFET_{ED}$ not only reduces the tunneling resistance by using smaller band-gap materials such as SiGe or Ge as a channel, but also suppresses the ambipolar current by forming the Si elevated drain on the channel [5] ($TFET_{ED}$ is one of the TFETs with vertical structures. In this study, $TFET_{ED}$ is used to represent the TFETs with various vertical structures). Though TFETs with vertical structures ($TFET_{VS}$) have been reported to suppress the ambipolar current and to enhance the I_{ON}, the previous works on the $TFET_{VS}$s have mainly focused on tunneling dynamics between source and channel. In this study, the effects of various pillar conditions such as pillar thickness (T_{pillar}), pillar height (T_{Si}), the ratio of channel length and pillar height, and the doping concentration of pillar on DC/AC characteristics of $TFET_{VS}$s are

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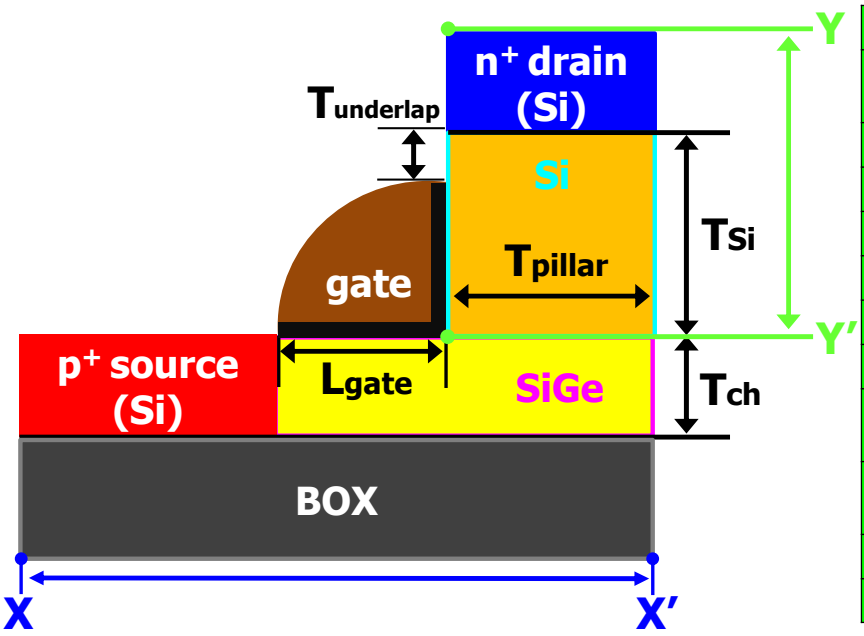

Lgate	30 nm
SiGe channel width	1 um
Tunderlap	20 nm
EOT	1.5 nm
Tch	20 nm
TSi	40 nm
Tpillar	90 nm
TBOX	100 nm
Source/Drain Doping	$1x10^{20}$ cm^{-3}
SiGe channel doping	$1x10^{15}$ cm^{-3}
Pillar doping	$1x10^{15}$ cm^{-3}
Gate WF	4.17 eV

Fig. 1. Device structure and physical parameters of TFETs used in the simulations.

rigorously investigated through mixed-mode device and circuit TCAD simulations.

II. Device Structure and Simulation Conditions

The cross-sectional structure of $TFET_{VS}$s used in this simulation study is shown in Fig. 1. In order to analyze the characteristics of $TFET_{VS}$s in an inverter configuration, mixed-mode device and circuit simulations are conducted by using Synopsys Sentaurus^{TM} which is especially suitable for accurate tunneling current calculation because it automatically defines tunneling path and mesh on the basis of the valence-band gradient [6-8]. The table of Fig. 1 shows the device parameters used in the simulations where a uniform doping profile is used for all the regions (namely, the source, the channel, and the drain regions) with an abrupt profile at the interfaces as applicable between them. Although the artificial doping profiles may result in the some disagreement in the current levels, this does not have much impact on our findings as the focus of this study is not on the exact values of currents but more on the changes of the device characteristics and the inverter switching characteristics by various pillar conditions. N-type TFET (nTFET) consists of p^+ source, p^- intrinsic channel, and n^+ drain, while the p^+ source/p^- channel/n^+ drain are replaced by n^+ source/n^- channel/p^+ drain in p-type TFET (pTFET). Gate leakage current is ignored, Fermi statistics is assumed, and nonlocal band-to-band tunneling (BTBT), drift-diffusion carrier transport, band-gap narrowing and Shockley-Read-Hall (SRH) recombination models are used.

To reflect accurate tunneling currents, tunneling model is first calibrated to experimental data for fabricated Si and $Si_{0.7}Ge_{0.3}$ TFETs. The Si TFET is fabricated on a (100) p-type silicon-on-insulator (SOI) wafer with 100 nm Si thickness on top of 375 nm buried oxide. The gate stack consists of 200 nm poly-Si layer and 3 nm SiO_2. After gate patterning, source and drain regions are defined through photolithography and implantation processes. BF_2 with dose of 8×10^{14} cm^{-2}, 7° tilt, and energy of 10 keV is used for source implantation. Drain implantation is also performed by using Arsenic (As) with the same condition. Dopant activation is implemented by rapid thermal process (RTP) at 900 °C during 5 sec. Also, the SiGe TFET is fabricated on a (100) p-type SOI wafer with 60 nm Si thickness. Epitaxial growing of the SiGe with Ge content of 30 percent and thickness of 40 nm is performed on the SOI wafer. Then, Si capping layer is grown on the SiGe channel to reduce defects at the interface between gate stack and SiGe channel (The capping layer is completely consumed to SiO_2 after gate oxidation). The following

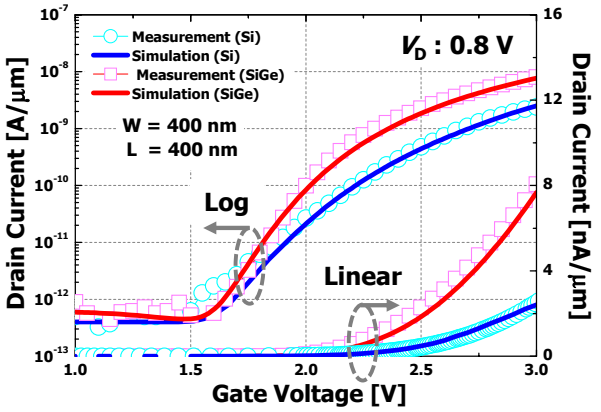

Fig. 2. Calibration results of simulated trasfer characteristics at drain bias (V_D) of 0.8 V. Tunneling model is calibrated to experimental data for the fabricated planar Si and SiGe TFETs.

fabrication processes are the same as those of the Si TFET.

To calculate BTBT generation rate (G) per unit volume in the uniform electric field, Kane's model is used [Eq. (1)] [9] and fitted parameters are as follows.

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right) \quad (1)$$

where F_0 = 1 V/m, P = 2.5 for indirect BTBT, A_{Si} = 4.0 × 10^{14} / A_{SiGe} = 3.1 × 10^{16} $cm^{-1}\cdot s^{-1}$ and B_{Si} = 9.9 × 10^6 / B_{SiGe} = 7.1 × 10^5 are Kane parameters of experimentally calibrated Si and SiGe materials respectively, and F is the electric field. Fig. 2 shows that the calibration results of the simulated transfer curves are well fitted to the measured data of the fabricated TFETs. Then, transient responses of $TFET_{VS}$ inverters with various pillar conditions are simulated for an input step voltage (V_{in}) with a peak-to-peak voltage of 0.8 V and a rise/fall time of 1 ns as can be seen in Fig. 6(c). Here, V_{DD} = 0.8 V and load capacitance (C_L) = 3 × 10^{-15} F are used.

III. Results and Discussion

TCAD simulations are performed to investigate the effects of various pillar conditions on DC characteristics of $TFET_{VS}$ devices and AC switching characteristics of $TFET_{VS}$ inverters. The device parameters of Fig. 1 are used in all the simulations except for changed conditions. Fig. 3(a) and (b) show that the drain current (I_D) of $TFET_{VS}$ becomes increased in both the transfer and

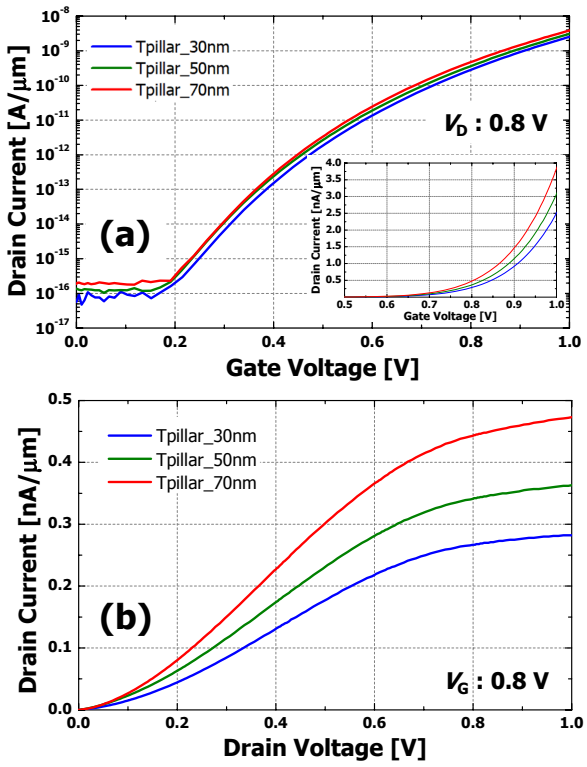

Fig. 3. (a) Transfer characteristics of n-type TFETs (nTFET) with various T_{pillar}s. The inset shows the transfer characteristics of linear scale, (b) Output characteristics of nTFETs with various T_{pillar}s.

output characteristics as the T_{pillar} gets thicker. This can be explained by the energy band diagrams of Fig. 4(a) and (b). The energy band diagrams show that gate voltage (V_G) controllability on the drain-side channel becomes weaker and drain voltage (V_D) has the stronger influence on the tunneling barrier between source and channel as the T_{pillar} gets thicker, similarly to drain-induced barrier lowering (DIBL) of MOSFETs. Thus, the tunneling current between source and channel gets increased due to the V_D-induced shorter tunneling length with the thicker T_{pillar}. To clarify the effects of the V_D on the source-side tunneling barrier and to optimize the pillar conditions, the pillar height (T_{Si}) and the doping concentration of the Si pillar are changed respectively. Fig. 5(a) indicates that the I_D gets decreased as the Si pillar has the higher doping concentration (p-type dopants are applied) because the depletion region formed at the interface between the drain and the Si pillar is reduced and thus the influence of the V_D on the source-side tunneling barrier becomes weaker with the higher doping concentration. Also, Fig. 5(b) shows that the I_D

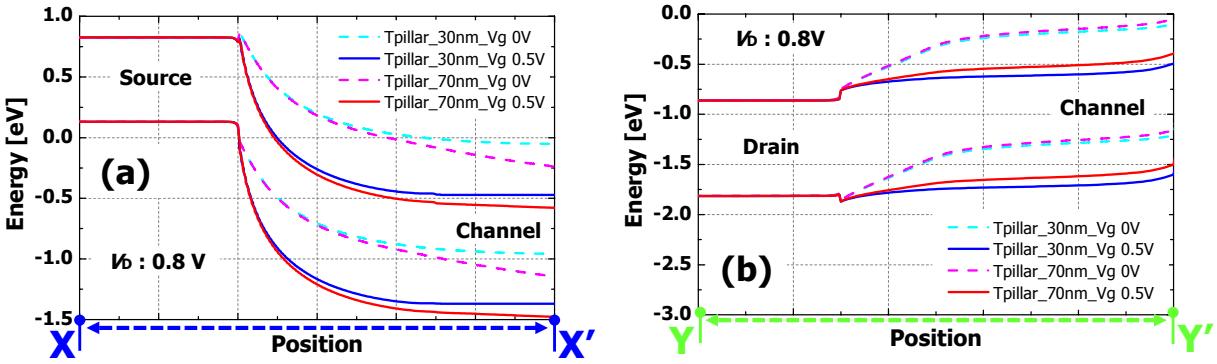

Fig. 4. (a) Energy band diagrams between source and channel in nTFETs with various T_{pillar}s, (b) Energy band diagrams between drain and channel in nTFETs with various T_{pillar}s.

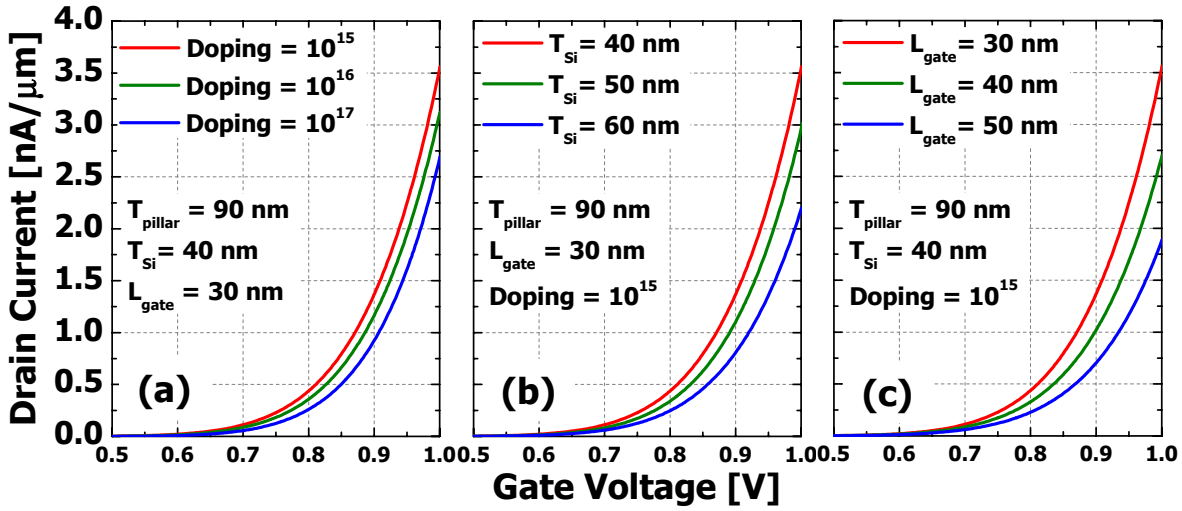

Fig. 5. The changes of transfer characteristics as a function of (a) doping concentration of pillar, (b) pillar height (T_{Si}), (c) length of SiGe channel (L_{gate}).

gets decreased with the higher pillar since the V_D has the weaker influence on the source-side tunneling barrier by the increased distance between the source and the drain. Additionally, the length of the SiGe channel (L_{gate}) is increased with the fixed pillar conditions of Fig. 1. Fig. 5(c) demonstrates that the I_D gets reduced as the L_{gate} becomes longer since the source is located further from the drain with the longer L_{gate} consistently with the results of the T_{Si} variation.

Furthermore, the V_G controllability on the drain-side channel can be verified by gate-to-drain capacitance (C_{GD})-V_G characteristics of $TFET_{VS}$. Fig. 6(a) shows that the C_{GD}-V_G curve gets positive-shifted as the T_{pillar} becomes thicker (As an example of the V_G controllability, the effects of the Tpillar on the C_{GD}-V_G curve are simulated.) This phenomenon can be explained as follows: For TFETs, the C_{GD} reflects the entire gate capacitance (C_{GG}) when the drain quasi-Fermi energy is well above the conduction band edge of the channel (namely, the occurrence of the drain-side channel inversion) [10]. As can be seen in the energy band diagrams of Fig. 4(b), the drain-side channel inversion occurs at larger V_G with the thicker T_{pillar} because the V_G has the weaker controllability on the drain-side channel by the thicker T_{pillar}, which leads to the positive-shifted C_{GD}-V_G curve. (Although both n-type and p-type TFETs are used for all the simulations, only the n-type branch is shown in the characteristics for simplicity.)

To investigate the effects of the increased I_D and the positive-shifted C_{GD}-V_G curve (namely, reduced C_{GD} throughout V_G transition) caused by the weaker V_G controllability on the drain-side channel on AC switching performances, the transient responses of $TFET_{VS}$ inverters with various T_{pillar}s are simulated as shown in

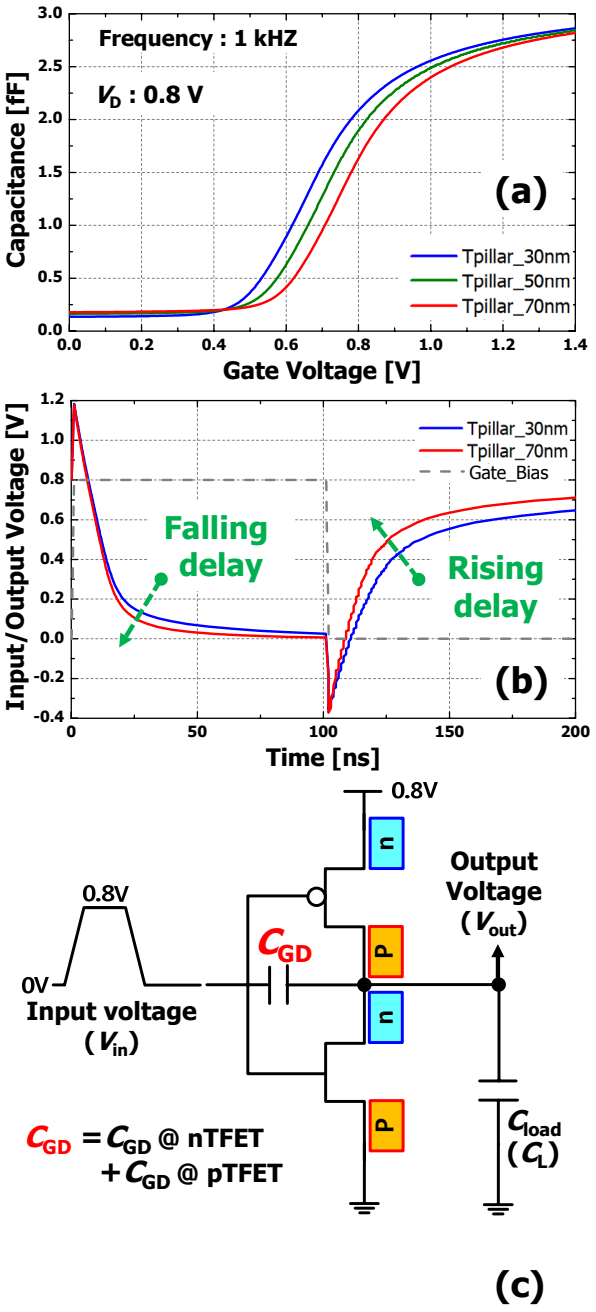

Fig. 6. (a) C_{GD}-V_G curves of nTFETs with various T_{pillar}s, (b) Transient responses of TFET inverters with various T_{pillar}s, (c) Circuit diagram of a TFET inverter and input signal.

the circuit diagram of Fig. 6(c) (L_{gate} = 30 nm, T_{Si} = 40 nm, and doping concentration of 1×10^{15} cm^{-3} are used in the inverter simulations considering the enhancement of I_D and the feasibility of fabrication even though the shorter L_{gate} and the lower T_{Si} result in more increased I_D.) As a result, Fig. 6(b) demonstrates that the output voltage (V_{out}) pre-shoot (signal peaking before transition) is slightly reduced and the falling/rising delay are significantly improved by the thicker T_{pillar}. This should be the result of the increased I_D and the reduced C_{GD} caused by the thicker T_{pillar} since it is widely accepted that the degraded V_{out} pre-shoot and the falling/rising delay of TFET inverters result from the combination of smaller current and larger C_{GD} as compared with those of MOSFETs [11, 12].

V. Conclusion

Mixed-mode device and circuit TCAD simulations are performed to investigate the effects of various pillar conditions on DC characteristics of $TFET_{VS}$ devices and AC switching characteristics of $TFET_{VS}$ inverters. As 1) the T_{pillar} is thicker, 2) the T_{Si} is increased, 3) the L_{gate} is longer, and 4) the doping concentration of the pillar is reduced, the I_D is increased in both the transfer and output characteristics due to the stronger influence of V_D on the tunneling barrier between source and channel. Moreover, the V_G controllability on the drain-side channel is verified by C_{GD}-V_G characteristics of $TFET_{VS}$. As a result, it is found that the weaker V_G controllability on the drain-side channel causes the positive-shifted C_{GD}-V_G curve. Through the transient responses of $TFET_{VS}$ inverters with various pillar conditions, the effects of the increased I_D and the positive-shifted C_{GD}-V_G curve caused by the weaker V_G controllability on AC switching performances are investigated thoroughly. Expectedly, it is confirmed that the V_{out} pre-shoot is reduced and the falling/rising delay are improved.

Acknowledgments

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