JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL. 21, NO. 4, AUGUST, 2021 ISSN(Print) 1598-1657
https://doi.org/10.5573/JSTS.2021.21.4.255 ISSN(Online) 2233-4866

A Non-binary C-R Hybrid DAC for 12 b 100 MS/s CMOS SAR ADCs with Fast Residue Settling

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Abstract—**This work proposes two versions of a 12 b 100 MS/s successive-approximation register (SAR) ADC based on a non-binary C-R hybrid DAC. The proposed DAC applies a non-binary weighted capacitor array to the 7 MSBs to meet the settling requirement of the DAC output and determines the remaining 5 LSBs using the reference voltages generated from a simple resistor string to reduce the DAC area significantly. The Version 1 ADC in a 28 nm CMOS adopts a synchronous SAR logic and a comparator with a tail capacitor and a reset switch to minimize power consumption. The Version 2 ADC in a 0.18 μm CMOS employs an asynchronous SAR logic with simple meta-stability correction logic to achieve high-speed operation. The Version 1 ADC which has an active die area of 0.042 mm^2 shows a maximum signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of 62.3 and 77.3 dB, respectively, consuming 1.3 mW with a 1.0 V supply voltage. The Version 2 ADC is based on a similar analog circuit topology, showing a maximum SNDR and SFDR of 60.1 and 73.5 dB, respectively, with an active die area of 0.30 mm^2, operating at a 1.8 V supply voltage.**

Index Terms—**Analog-to-digital converter (ADC), non-binary weighted capacitor array, successive approximation register (SAR), asynchronous, low power comparator**

Manuscript received Apr. 6, 2021; reviewed Jun. 19, 2021; accepted Jul. 5, 2021
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I. INTRODUCTION

With the expansion of new mobile communication systems such as 5G networks and wearable devices, there has been an increase in demand for mobile devices based on such systems [1-3]. These mobile devices require analog-to-digital converters (ADCs) that can achieve a resolution of over 10 b at a sampling rate exceeding 100 MS/s while maintaining high power efficiency and small chip area when the speed is adjusted as needed. To meet these stringent requirements for the ADCs, much research has been conducted on the development of low-power, small-area successive-approximation register (SAR) ADCs. However, SAR ADCs are typically limited in their application due to the difficulty in achieving the required digital-to-analog converter (DAC) output settling time at high-speed operation [4-6]. To overcome this limitation in SAR ADCs, research is being conducted on time-interleaving and 2b/cycle techniques. However, these techniques require the use of additional circuit blocks, thereby reducing efficiency with respect to power consumption and chip area. While some correction schemes can relax the DAC settling requirement for high-speed operation, commonly employed methods include non-binary search algorithm and binary-scaled error compensation. Compared to the binary-scaled error compensation scheme, the non-binary search algorithm could correct a relatively higher number of bit error decisions with the same number of unit capacitors [7]. This work thus proposes 12 b 100 MS/s SAR ADCs based on a non-binary weighted DAC to shorten the required DAC output settling time.

The proposed SAR ADC architecture in this work is

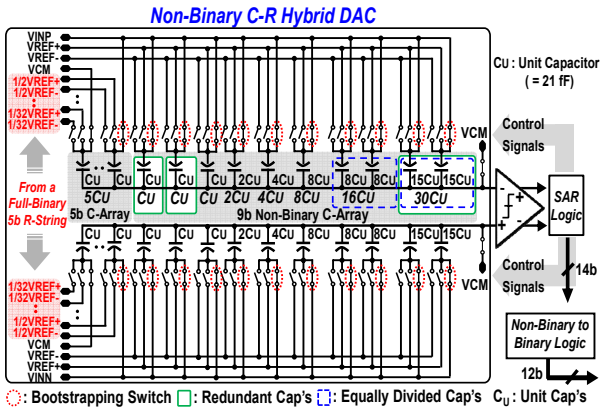

Fig. 1. Proposed 12 b 100 MS/s SAR ADC employing a non-binary weighted C-R hybrid DAC.

shown in Section II. Detailed circuits are described in Section III, while the measurement results are discussed in Sections IV and V.

II. Proposed SAR ADC Topology

The overall structure of the proposed ADC is illustrated in Fig. 1. The proposed ADC consists of a non-binary weighted C-R hybrid DAC, a comparator, a SAR logic block, and an encoder that converts a 14 b non-binary digital code into a 12 b binary digital code.

The C-R hybrid DAC shown in Fig. 1 is again composed of a 9 b non-binary weighted capacitor-array (C-array) and a 5 b C-array, where C_U represents a unit capacitor of 21 fF. The 9 b C-array is used to decide the 7 most significant bits (MSBs). In this structure, 30 C_U's are employed, compared to the typical nominal binary weighted 32 C_U's, with 2 C_U's as redundant capacitors to alleviate the settling requirement of the DAC output with error correction [8-10]. The remaining 5 least significant bits (LSBs) are decided by five unit capacitors in the 5 b array, combined with 10 reference voltages obtained from a simple resistor string [11]. Since the proposed DAC employs a total of only 68 capacitors rather than the 4096 required for a full binary weighted 12 b resolution, the required die area for the SAR ADC is significantly reduced, even when taking into account the extra area occupied by the noncritical simple resistor string. The proposed ADCs are implemented in two versions with different processes. The Version 1 ADC in a 28 nm CMOS employs a synchronous SAR logic circuit with a low power dynamic comparator to

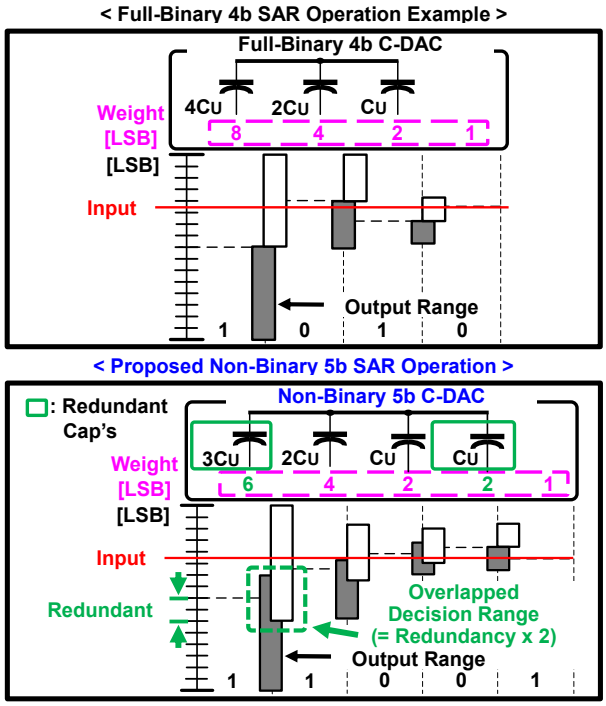

Fig. 2. SAR operation based on binary and non-binary weighted DACs.

minimize power consumption. Meanwhile, The Version 2 ADC in a 0.18 μm CMOS employs an asynchronous SAR logic circuit for the same 100 MS/s target operation for a relatively long channel. The Version 2 ADC also proposes a simple meta-stability correction logic circuit to remove the meta-stable state of the comparator.

III. Circuit Description

1. Non-binary Weighted DAC

An example of the SAR operations based on both the binary and non-binary weighted DACs used to determine a 4 b digital output is illustrated in Fig. 2. The decision range of the binary weighted DAC is not overlapped, while that of the non-binary weighted DAC is overlapped by the redundancy generated from the two separate redundant capacitors, 3 C_U and 1 C_U [8-10].

The signal settling range of the non-binary weighted DAC can be considerably increased in proportion to the overlapped range, as shown in the waveform of Fig. 3, while the output voltage of the binary weighted DAC needs to be settled within a maximum 1/2 LSB of the ideal settling level. The required settling times of the

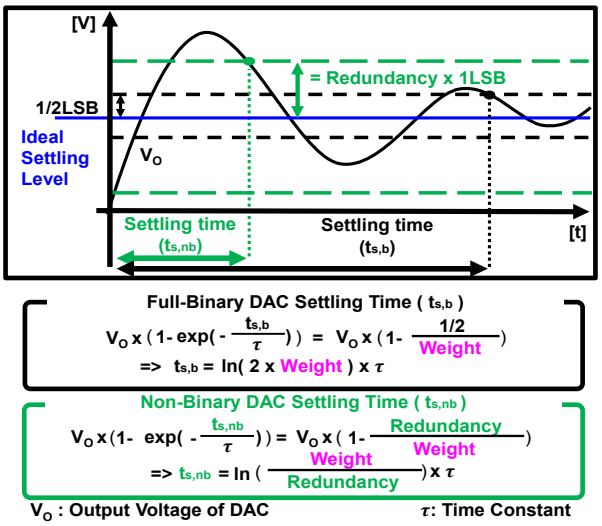

Fig. 3. Comparison and estimation of the DAC settling time.

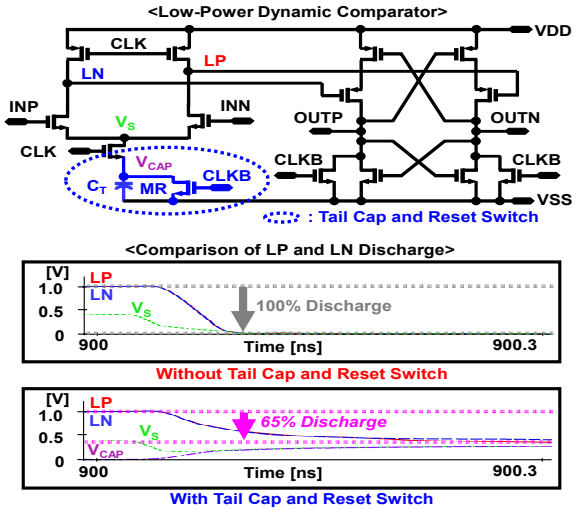

Fig. 4. Low power dynamic comparator of Version 1 ADC.

DAC output can be calculated by the equations in boxes of Fig. 3, where '$t_{s,b}$' and '$t_{s,nb}$' represent the output settling time in the full-binary and non-binary DAC, respectively.

The elements 'τ', 'Weight', and 'Redundancy' are the time constant, the weighted value of the CDAC capacitor, and the overlapped decision range of the non-binary weighted DAC, respectively. In the conventional DAC, the maximum 'Weight' is 2048 LSB for the MSB capacitor and the estimated maximum $t_{s,b}$ is 8.32 τ. However, the proposed DAC has a 'Redundancy' of 128 LSB, generated by the 2 C_Us, and the 'Weight' of the MSB capacitor is 1920 LSB. The estimated $t_{s,nb}$ of the proposed DAC is 2.71 τ, with a reduction factor of 67 %, while the maximum output settling time does not occur in the first conversion cycle. Instead, the maximum output settling time in the proposed DAC is 4.85 τ, which occurs in the eighth conversion cycle, where the 'Weight' is 64 LSB and there is no more 'Redundancy'. As a result, the estimated total sum of the output settling time in the conventional DAC is 54.07 τ, compared to 29.74 τ in the proposed DAC. Therefore, the maximum settling time and the total sum of the settling time of the DAC output voltage are dramatically reduced by 42% and 45%, respectively, in the proposed non-binary weighted DAC.

2. Low Power Dynamic Comparator

To achieve low power consumption, a dynamic comparator with a tail capacitor, C_T, and a reset switch, MR, is employed in the Version 1 ADC [12, 13]. As shown in Fig. 4, the charged voltages of the LN, LP, and VS nodes in the conventional comparator are completely discharged to 0 V. However, the charged voltages of the same three nodes in the comparator are discharged to approximately 65% of the initial values. The comparator thus significantly improves the power efficiency and operating speed of the ADC.

3. Asynchronous SAR Logic

The Version 2 ADC in a 0.18 μm CMOS adopts an asynchronous SAR logic to eliminate the idle periods between conversion steps for the same 100 MS/s high conversion target as the Version 1 ADC which is applied in a 28 nm CMOS [14]. In addition, since the conversion speed of the SAR ADC tends to be limited by the SAR loop delay time, the delay time-reduced SAR logic adopted in the Version 2 ADC is able to directly control the CDAC switch from the REG output without any extra DAC switching logic. The asynchronous SAR logic with its specific timing diagram is illustrated in Fig. 5.

As soon as the logic status of the sampling clock 'FSB' and the reset clock 'RST' changes, the comparator is ready to compare two 'CDAC' outputs with the ready clock 'RDY' set to 'high', starting a bit conversion. In

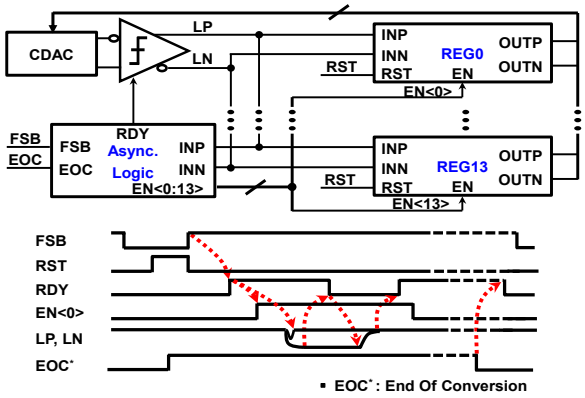

Fig. 5. Asynchronous SAR logic of Version 2 ADC.

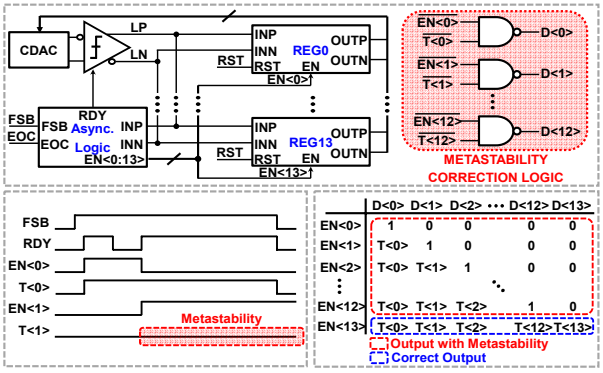

Fig. 6. Example of the meta-stability correction logic function.

succession, the register-enable clock ‘EN<0>’ is set to ‘high’ and selects ‘REG0’ to store the corresponding comparator output. Immediately after the bit conversion is completed, the compared output ‘LP, LN’ resets the ‘RDY’ clock to turn off the comparator, and accordingly, ‘LP, LN’ is also reset to ‘high’. The proposed SAR logic operates asynchronously during the total 14 b conversion cycles [15]. After the last 14th bit conversion, the ‘EOC’ clock is set to ‘low’ indicating that the overall 14 b conversion is completed.

4. Proposed Meta-stability Correction Logic

With the significantly reduced SAR conversion time due to the asynchronous operation, a simple meta-stability correction logic is also proposed in the Version 2 ADC. The proposed meta-stability correction logic forces all the lower bits from the possible meta-stable bit to be set to ‘100...’ as illustrated in the example of Fig. 6.

When the comparator operates without any meta-stable state in all conversion cycles, the digital code ‘D<0:13>’ is generated by the register outputs ‘T<0:13>’. However, if a meta-stable state occurs in the comparator, the corresponding meta-stable bit is considered as ‘1’, and the remaining bits are considered as ‘0’. As a result, all bits including the meta-stable bit are considered as ‘100...0’. For example, as shown in Fig. 6, if the first bit ‘D<0>’ is ‘1’ and the meta-stable state occurs in the second conversion cycle, the corresponding register output ‘T<1>’ and the register enable clock ‘EN<1>’ are set to ‘low’ and ‘high’, respectively. Therefore, the digital code ‘D<1>’ is determined as ‘1’ through the NAND gate that receives ‘T<1>’ and ‘EN<1>’ as inputs.

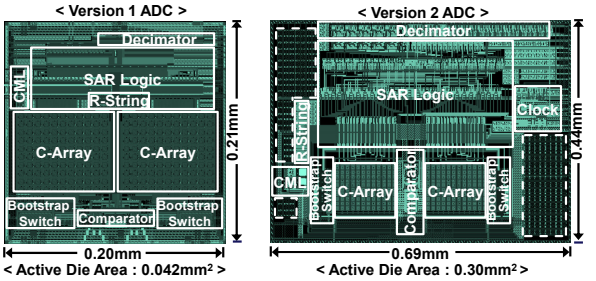

Fig. 7. Chip layout of the proposed prototype ADCs.

Meanwhile, all the lower bits from ‘D<2>’ are set to ‘00...0’ based on the remaining NAND gates and the register enable clock. As a result, the 12-bit digital code is considered as ‘110000000000’.

IV. Measurement Results

The proposed non-binary DAC-based 12 b 100 MS/s ADCs are implemented in two versions with 28 nm and 0.18 μm CMOS processes. The active die area of the two prototype ADCs is 0.042 mm^2 and 0.30 mm^2, as shown in Fig. 7, respectively. The Version 1 ADC consumes 1.3 mW with a 1.0-V supply voltage while the Version 2 ADC consumes 11.3 mW with a 1.8-V and 1.7-V for analog and digital supply voltage, respectively. The power breakdown is detailed in Fig. 8.

The measured differential non-linearity (DNL) and integral non-linearity (INL) of the prototype ADCs are shown in Fig. 9. The DNL and INL of the Version 1 ADC are within 0.67 LSB and 1.55 LSB, while the DNL and INL of the Version 2 ADC are 0.66 LSB and 1.65 LSB, respectively.

The measured signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of the

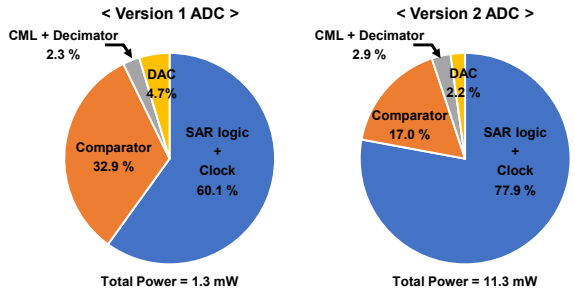

Fig. 8. Power breakdown of the proposed prototype ADCs.

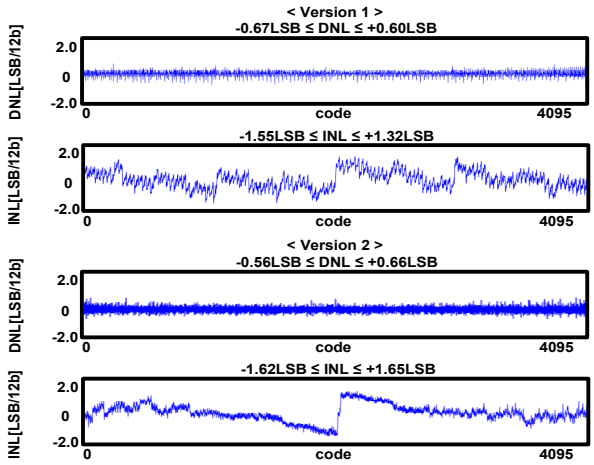

Fig. 9. Measured static performance of the prototype ADCs.

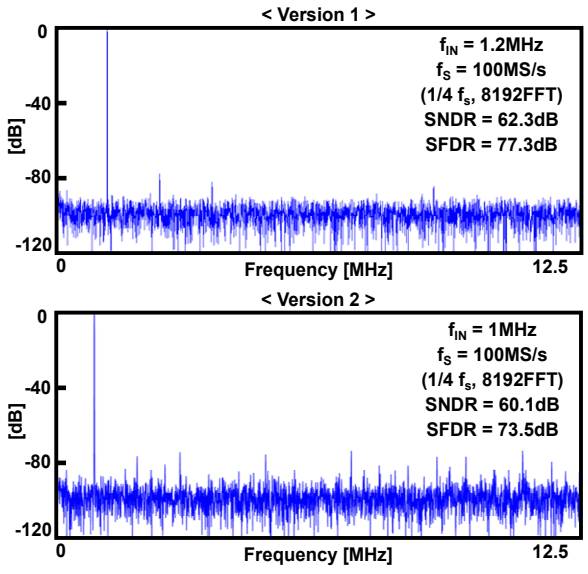

Fig. 10. Measured FFT spectrum of the prototype ADCs with a decimation factor of 4.

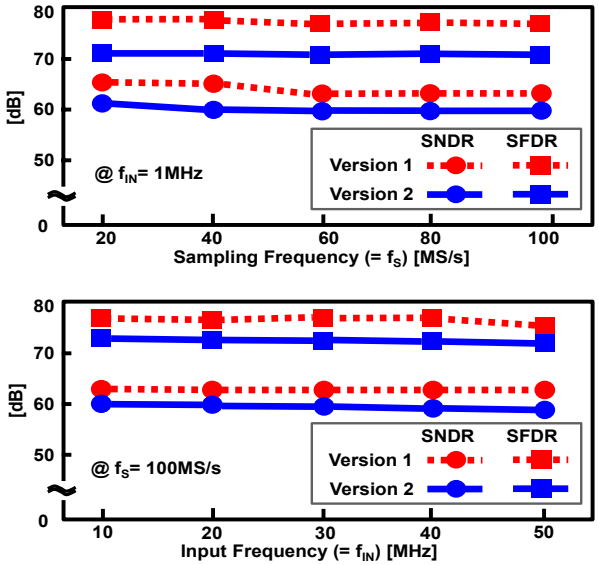

Fig. 11. Measured dynamic performance of the prototype ADCs.

Table 1. Performance comparison of the Version 1 ADC

	IET'20 J.-S. Park [11]	TCAS-II'20 Y.-J. Roh [16]	TCAS-II'19 Y. Chung [17]	**This work (Ver. 1)**
Process [nm]	180	40	65	**28**
Resolution [bits]	12	12	12	**12**
Speed [MS/s]	50	120	100	**100**
Analog Supply [V]	1.8	1	1.2	**1.0**
Digital Supply [V]				
Power [mW]	4.7	1.9	1.9	**1.3**
SNDR [dB]	64.3	60.33	61.5	**62.3**
SFDR [dB]	74.7	72.9	81	**77.3**
Calibration	No	Yes	Yes	**No**
Area [mm^2]	0.17	0.0128	0.053	**0.042**
FoM [fJ/Con.]	70.6	18.7	19.6	**12.2**

prototype ADCs are plotted in Fig. 10 and 11. The Version 1 ADC shows maximum SNDR and SFDR of 62.3 dB and 77.3 dB, while the Version 2 ADC shows maximum SNDR and SFDR of 60.1 dB and 73.5 dB, respectively, at an operating speed of 100 MS/s and an input frequency of 1 MHz. When the input frequency is increased to the Nyquist frequency at 100 MS/s, the SNDR and SFDR of the Version 1 ADC are maintained above 61.5 dB and 76.3 dB, while the SNDR and SFDR of the Version 2 ADC are maintained above 58.4 dB and 72.1 dB, respectively.

The performance of the Version 1 ADC is summarized and compared with previously reported ADCs in Table 1.

V. CONCLUSIONS

This work proposes 12 b 100 MS/s SAR ADCs based on a non-binary C-R hybrid DAC for high-speed residue settling. The proposed ADCs are implemented in two versions based on different processes. The Version 1 ADC employs a synchronous SAR logic and a low power dynamic comparator to minimize power consumption. The Version 2 ADC employs an asynchronous SAR logic with simple meta-stability correction logic to achieve high-speed operation. Although the power and the die area of the Version 2 ADC are much larger than the Version 1 ADC, primarily, due to two substantially different CMOS processes of 28 nm and 0.18 μm, the Version 2 ADC properly operates at a high-speed of 100 MS/s even in a 0.18 μm CMOS process. Based on the benefits of scaled-down process, the Version 1 ADC with a 28 nm CMOS process achieves a competitive figure-of-merit (FoM) of 12.2 fJ/conversion-step.

ACKNOWLEDGMENTS

This work was supported by Samsung Electronics Co., Ltd (IO201210-08008-01), the IDEC of KAIST, and the MSIT under the ITRC program (IITP-2021-2018-0-01421) supervised by the IITP.

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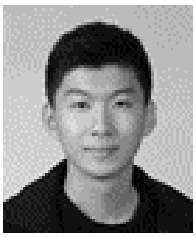

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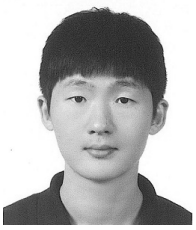

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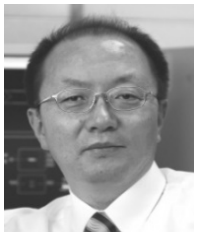

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