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A Wideband Sub-GHz Receiver Front-end Supporting High Sensitivity and Selectivity Mode

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***Abstract*—A low noise and highly linear wideband RF front-end circuit for sub-GHz Internet of Things (IoT) applications is proposed. The proposed front-end is composed of a broadband single-ended LNA, a wideband differential LNA employing thermal noise cancellation technique, and an in-phase and quadrature (I/Q) linearized harmonic rejection mixer (HRM). Depending on the interference environment, the proposed front-end supports two operation modes having high sensitivity and selectivity performance by enabling or disabling the first building block of the single-ended LNA. At high sensitivity mode, the front-end shows a voltage gain (A_v) of greater than 38 dB, a noise figure (NF) of less than 2.1 dB, an input-referred third-order intercept point (IIP3) of greater than -23 dBm, and an input-referred second-order intercept point (IIP2) of greater than +15 dBm in the sub-GHz frequency band. Concerning for high selectivity mode, it achieves an A_v of greater than 22.5 dB, a NF of less than 4.7 dB, an IIP3 of greater than –6.8 dBm, and an IIP2 of greater than +50 dBm over the same operating frequency range.**

***Index Terms*—CMOS, front-end, harmonic rejection mixer, low noise amplifier (LNA), sub-GHz, wideband**

I. INTRODUCTION

Internet of Things (IoT) has become an emerging and fast-growing heterogeneous network that can interconnect a variety of devices, people, data, and processes for a wide range of applications. Recently, sub-GHz low power wide area network (LPWAN) technologies such as SigFox, long-range wide area network (LoRaWAN), narrowband IoT (NB-IoT), and long-term evolution (LTE)-M have been introduced to ensure a long transmission range of more than multiple kilometers with low power consumption.

The front-end circuit for sub-GHz IoT applications must be capable of handling signals with broadband input frequencies ranging from 50 MHz to 900 MHz in order to support multiple LPWAN technologies with a single hardware. This wideband nature of input signals can cause the odd local oscillator (LO) harmonic mixing problem. Because the undesired channels located at LO harmonic frequencies are aliasing into the wanted channel and thus this directly degrades signal-to-noise ratio (SNR) of the receiver, the harmonic rejection functionality is required absolutely for sub-GHz IoT front-end. In addition, the front-end should provide a sufficiently high voltage gain and a low noise figure (NF) to satisfy the stringent sensitivity requirement for various sub-GHz IoT standards. Depending on the interference environment, it also should have high linearity represented by input-referred IP3 and IP2 (IIP3 and IIP2) because the second- and third-order intermodulation distortion (IMD2 and IMD3) caused by the multiple interferers in a crowded sub-GHz spectrum can fall at the same frequency of the desired channel.

In this paper, a low noise and highly linear wideband

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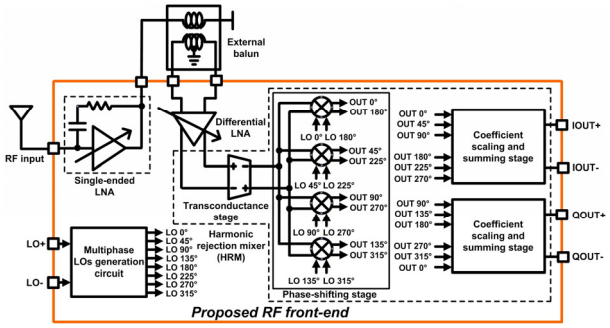


Fig. 1. Block diagram of the proposed RF front-end for sub-GHz IoT applications.

CMOS RF front-end is designed for sub-GHz IoT applications. The single-ended resistive feedback LNA, the wideband differential LNA employing thermal noise cancellation, and the in-phase and quadrature (I/Q) harmonic rejection mixer (HRM) employing IMD3 cancellation are designed in a 0.18-μm CMOS technology.

II. Circuit Implementation

Fig. 1 shows the block diagram of the proposed RF front-end for sub-GHz IoT applications. The LNA is composed of the single-ended resistive feedback LNA (SLNA) and differential noise canceling common gate (CG) LNA (DLNA). At high sensitivity mode, the SLNA is operated as the first amplification stage of the receiver to compensate the power loss of external wideband balun and achieve sufficiently high voltage gain. This leads to excellent sensitivity performance of the receiver. On the other hand, for high selectivity mode, the operation of SLNA and DLNA is dominated by IIP2 performance because the LNA with single-ended input and output shows very poor IIP2. It was reported in [1] that the required IIP2 of the wideband LNA exceeds more than +90 dBm without filtering under the condition that 1.8 GHz GSM interferer and 2.4 GHz WLAN interferer generate IMD2 in the wanted frequency of 600 MHz. Although some out-of-band (OOB) rejection characteristic of the filter can relax the required specification, it is almost impossible for the single-ended LNA to achieve this level of IIP2 performance.

Several linearization techniques to improve IIP2 of the single-ended LNA have been devised in [2-4], however, the amount of improvement is very sensitive to process,

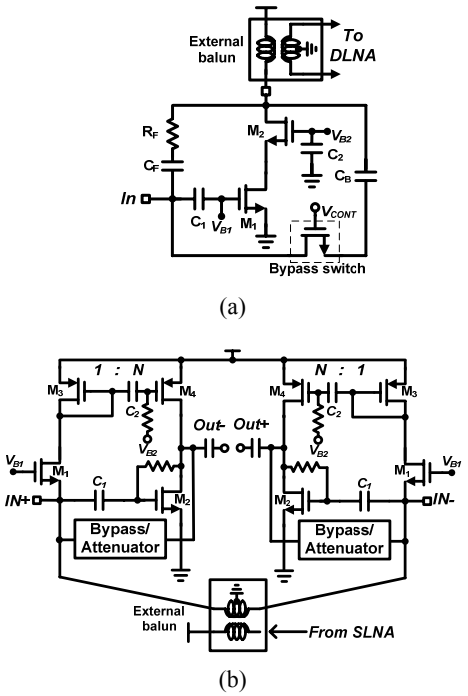


Fig. 2. (a) Schematic of the wideband single-ended LNA, (b) schematic of the wideband noise canceling differential LNA.

temperature, and voltage (PVT) variations. The complex calibration circuit to compensate PVT variations should be integrated with LNA core circuit, and this increases the hardware complexity and power consumption of the receiver. As a result, it is desirable to adopt the fully differential LNA having an excellent IIP2 as the first amplification stage of the receiver at high selectivity mode. In this work, concerning for high selectivity mode, the SLNA is powered down and it is bypassed into the DLNA without any amplification. Namely, the DLNA becomes the first amplification stage of the receiver. One of the concerns in this scheme is that the sensitivity degradation resulting from the additional power loss caused by by-pass switch and external wideband balun is inevitable at the price of high IIP2 performance. Fortunately, this is not significant because the sensitivity specification at high selectivity mode is relaxed than high sensitivity mode. In conclusion, by selecting the SLNA or the DLNA as the first amplification stage according to the mode of the receiver, the stringent requirements of sensitivity and selectivity for sub-GHz IoT receivers can be satisfied simultaneously.

For the SLNA of Fig. 2(a), the resistive feedback LNA is chosen because of its wide input impedance matching, low NF, and reasonable voltage gain with the advantage

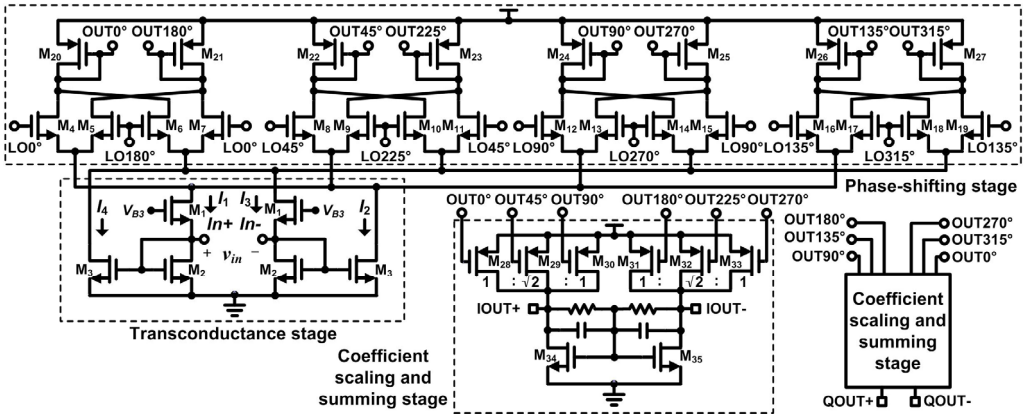


Fig. 3. Schematic of the proposed HRM composed of a transconductance stage, a phase-shifting stage, and two coefficient scaling and summing stages for I and Q path.

of using no external input matching components. For linearity, the feedback LNA provides good linearity because the negative feedback reduces distortion components by a factor of loop gain [5]. The external transformer is employed as the output load of the SLNA, and it operates as an RF choke to provide a sufficiently high gain and ensure a good linearity. In addition, it converts a single-ended signal into a differential signal for the DLNA. The use of an external transformer is inevitable because it is almost impossible to implement a broadband on-chip transformer working over the entire frequency bands from 50 MHz to 900 MHz due to the limitation of silicon area and power loss.

Fig. 2(b) shows the proposed broadband LNA employing thermal noise cancellation based on current amplification. By adopting the structure combining the CG amplifier (M_1) with the common source (CS) amplifier (M_2) thorough the current mirror, the dominant noise source from M_1 is cancelled out at the LNA output. This is when total transconductance ($g_{m1}N$) of the CG transistor with current amplification is equal to the transconductance (g_{m2}) of the CS transistor. The wideband input impedance matching (Z_{IN} = $2/g_{m1}$) is easily obtained by the CG amplifier. In addition, the proposed LNA has relatively high IIP3 due to current amplification, which can eliminate voltage-to-current (V-I) conversion process resulting in nonlinearity. The adopted current mirror in this work is on the basis of a modified current mirror configuration. In the modified current mirror, instead of dc coupling, two current mirror transistors M_3 and M_4 are ac-coupled through the capacitor C_2. Because the width of the transistor M_4 can be increased under allowed gain bandwidth without dc current amplification, the modified current mirror shows higher current mirror ratio $N = (W/L)_4/(W/L)_3$ with low dc power consumption compared to conventional current mirror.

Fig. 3 shows the schematic of the HRM composed of a transconductance stage, a phase-shifting stage, and two coefficient scaling and summing stages for in-phase (I) and quadrature-phase (Q) path. Because the linearity burden of the RF front-end lies in the down-conversion mixer, it is important to design a highly linear wideband down-conversion HRM. In order to improve the linearity of the mixer in wideband without additional power consumption, the micro-mixer topology with the CG input stage employing IMD3 cancellation technique is adopted as shown in Fig. 3. The IMD3 current ($I_{t.3rd}$) of the linearized input transconductor in Fig. 3 can be expressed as

$$\begin{aligned} I_{t.3rd} &= I_1 + I_2 - (I_3 + I_4) \\ &= \frac{1}{24}\left(g_{m1}{}^{(2)} - g_{m2}{}^{(2)} + g_{m3}{}^{(2)}\right) v_{in}^3 \end{aligned} \tag{1}$$

where v_{in} is the small signal input voltage of the mixer and $g_m{}^{(2)}$ is the second derivative of the transconductance g_m. In order to obtain high IIP3, the magnitude of $g_{m1}{}^{(2)}$-$g_{m2}{}^{(2)}$+ $g_{m3}{}^{(2)}$ should be minimized by choosing the proper size and dc bias of the transistors M_1, M_2, and M_3 [6].

The 45° phase-shifted multiphase LO signals drives the HRM. The four switching mixers to generate I and Q baseband signals is used in the HRM. The phase-shifting stage plays the role of the phase rotation of an input

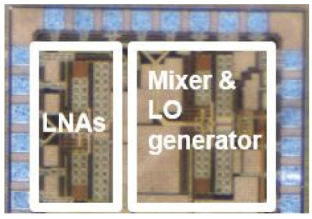


Fig. 4. Chip photograph of the proposed RF front-end.

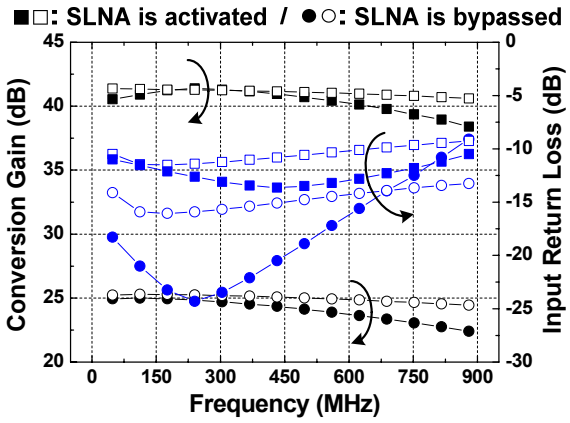
signal using 45° phase-shifted LO signals as well as down-conversion through four individual switching mixers. In the coefficient scaling and summing stage, three phase-shifted baseband signals down-converted from RF bands are combined with weighted size ratio of 1:√2:1 through current mirror pairs (M_{20} and M_{28} : M_{22} and M_{29} : M_{24} and M_{30}). The coefficient scaling and summation in the baseband domain reduces the gain mismatch compared to that in the RF domain of [7].

III. Measurement Results

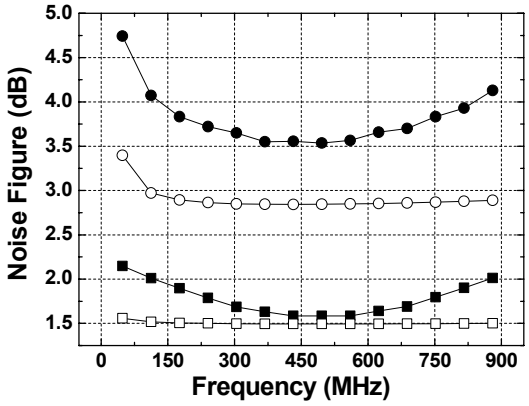
The proposed RF front-end was fabricated in a 180 nm RF CMOS technology. Fig. 4 shows a photograph of the proposed RF front-end. The chip size is 1 mm × 0.7 mm, including pads. The proposed RF front-end including LO generation circuit draws 11.6 mA for high selectivity mode and 15.6 mA for high sensitivity mode from a 1.8 V supply voltage, respectively.

Fig. 5 shows the simulated and measured conversion gain (A_v), input return loss (S_{11}), NF, IIP3, and IIP2 of the proposed RF front-end when the SLNA is activated and bypassed, respectively. The filled and blank symbols denote the measurement and simulation results, respectively. The simulated IIP2 result is omitted because it depends on the amount of mismatch of the differential structure in the layout. The reported NF is the double-sideband NF, and the two tone spacing is 1 MHz for the linearity test.

At high sensitivity mode where the SLNA is enabled, the RF front-end shows an A_v of greater than 38 dB, a NF of less than 2.1 dB, an IIP3 of greater than -23 dBm, and an IIP2 of greater than +15 dBm in the measurement. Concerning for high selectivity mode where the SLNA is powered down, the RF front-end achieves an A_v of greater than 22.5 dB, a NF of less than 4.7 dB, an IIP3 of greater than –6.8 dBm, and an IIP2 of greater than +50 dBm in the measurement. On the whole, the



(a)



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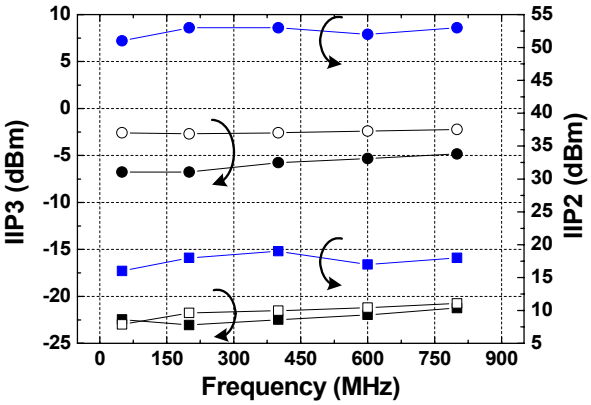

(c)

Fig. 5. Simulated and measured (a) conversion gain (A_v) and input return loss (S_{11}), (b) NF, (c) IIP3 and IIP2 of the proposed RF front-end. The filled and blank symbols denote the measurement and simulation results, respectively. The simulated IIP2 result is omitted because it depends on the amount of mismatch of the differential structure in the layout.

measurement result is well matched to the simulation result. Compared to the simulation result, due to a narrower bandwidth of the front-end circuit, the

Table 1. Performance Summary and Comparison with Traditional Front-end Circuits for Sub-GHz IoT Receivers

	[8] CICC'09	[9] JSSC'12	[10] TCAS-I'14	[11] TCAS-II'17	This Work (Sensitivity)	This Work (Selectivity)
RF Frequency (MHz)	54 – 862	30 – 2400	54 – 882	50 – 880	50 – 900	
Conversion Gain (dB)	< 107	> 66	> 21.5	> 35	> 38	> 22.5
NF_{DSB} (dB)	5 – 8.5	5 – 8	3.3 – 4.1	3 – 3.5	1.6 – 2.1	3.5 – 4.7
IIP3 (dBm)	-16 @ 0.8 GHz	-11 @ 0.6 GHz	-5 @ 0.8 GHz	-17.5 @ 0.8 GHz	-21 @ 0.8 GHz	-5 @ 0.8 GHz
IIP2 (dBm)	NA	+13 @ 0.6 GHz	+32 @ 0.8 GHz	NA	+18 @ 0.8 GHz	+53 @ 0.8 GHz
3rd LO HRR (dB)	43 @ 0.9 GHz	43 @ 0.6 GHz	NA	52 @ 0.1 GHz	57 @ 0.25 GHz	
LNA Topology	Single-ended	Single-ended	Differential	Differential	Single-ended	Differential
Power Consumption (mW)	(1)77.4 @ 1.8 V	30 – 44.4 @ 1.2 V	(1)40.5 @ 1.5 V	25.2 @ 1.8 V	28 @ 1.8 V	21 @ 1.8 V
Process Technology (CMOS)	180-nm	90-nm	130-nm	180-nm	180-nm	

(1) Power consumption excluding multi-phase LO generation circuit

measured A_v slightly drops as the operating frequency increases. Because the gain of the DLNA is not high enough to suppress the noise contribution of the following HRM, the difference between the simulated and measured NF at high selectivity mode becomes slightly higher than that at high sensitivity mode. In case of the measured S_{11}, the proposed front-end shows a S_{11} of lower than -10 dB over the entire operating frequency bands.

Fig. 6 presents the measured 3rd LO harmonic rejection ratio (HRR) of the proposed front-end. The LO signal of 250 MHz, desired input signal of 251 MHz, and undesired interferer of 751.1 MHz were applied to the input of the receiver. Then, the fundamental component of 1 MHz and 3rd LO harmonic mixing component of 1.1 MHz were detected for the measurement of the 3rd LO HRR. The measured 3rd LO HRR is 57.3 dBc without any calibration. Fig. 7 shows the measured 3rd and 5th LO HRR over the operating frequency range. The front-end circuit achieves quite high HRR performance ranging from -55 dBc to -60 dBc due to accurate coefficient scaling and summation in the baseband domain through current mirrors.

In Table 1, experimental results are summarized and compared to the traditional front-end circuits for sub-GHz IoT receivers. The proposed front-end shows an excellent NF at high sensitivity mode and linearity (IIP3 and IIP2) at high selectivity mode with lower power consumption in comparison with the conventional front-end circuits.

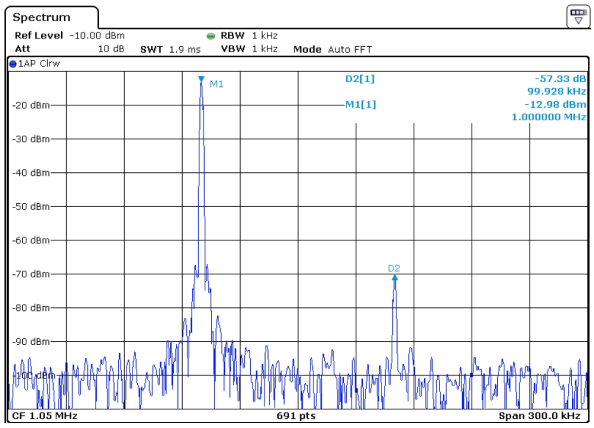

Fig. 6. Measured 3rd LO harmonic rejection ratio (HRR).

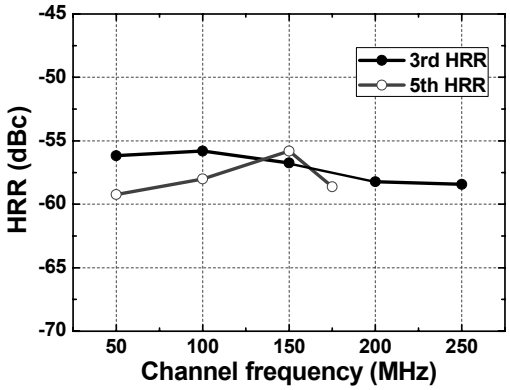

Fig. 7. Measured 3rd and 5th LO HRR over the operating frequency range.

IV. CONCLUSIONS

A low noise and highly linear wideband RF front-end with the harmonic rejection mixer is implemented as a part of the low power sub-GHz IoT receiver. Depending on the interference environment, the proposed front-end supports two operation modes having high sensitivity and selectivity performance by enabling or disabling the first building block of the single-ended LNA. By selecting the SLNA or the DLNA as the first amplification stage according to the mode of the receiver, the stringent requirements of sensitivity and selectivity for sub-GHz IoT receivers can be satisfied simultaneously.

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REFERENCES

[1] S. C. Blaakmeer *et al.*, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[2] D. Manstretta, "A broadband low-power low-noise active balun with second-order distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 407–420, Feb. 2012.

[3] S. Kim *et al.*, "A 50-MHz–1-GHz 2.3-dB NF noise-cancelling balun-LNA employing a modified current-bleeding technique and balanced loads," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 546–554, Feb. 2019.

[4] D. Im *et al.*, "A High IIP2 Broadband CMOS Low-Noise Amplifier With a Dual-Loop Feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2068-2079, July 2016.

[5] J. Kim *et al.*, "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 9, pp. 2340–2351, Sep. 2010.

[6] Y.-W. Lim *et al.*, "A highly linear wideband up-conversion differential CMOS micromixer using IMD3 cancellation for a digital TV tuner IC," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 2, pp. 89-91, Mar. 2009.

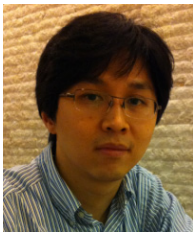
[7] M. Gupta *et al.*, "A 48-to-860 MHz CMOS direct-conversion TV tuner," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, San Francisco, CA, Feb. 2007, pp. 206-207.

[8] J. Kim *et al.*, "A 54–862 MHz CMOS direct conversion transceiver for IEEE 802.22 cognitive radio applications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 255–258.

[9] M. Kitsunezuka *et al.*, "A 30-MHz–2.4-GHz CMOS receiver with integrated RF filter and dynamic-range-scalable energy detector for cognitive radio systems," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1084–1093, May 2012.

[10] D. Im *et al.*, "A wideband digital TV receiver front-end with noise and distortion cancellation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 562–572, Feb. 2014.

[11] D. Im *et al.*, "A TV receiver front-end with linearized LNA and current-summing harmonic rejection mixer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 3, pp. 269–273, Mar. 2017.



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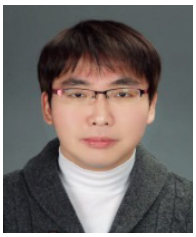

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