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All-directional Electrostatic-discharge Protection Circuit with High Area-efficiency

Kyoung-Il Do, Byung-Seok Lee, Seung-Hoo Jin, and Yong-Seo Koo

Abstract— **This paper proposes a design for a whole-chip all-directional electrostatic-discharge (ESD) protection circuit using a resistor-capacitor (RC) lateral insulated-gate bipolar transistor (LIGBT)-based 12 V power clamp and a silicon-controlled rectifier (SCR)-based 12 V input/output (I/O) clamp. The RC LIGBT-based power clamp detects pulses through an ESD detection circuit and applies a bias to the gate. Therefore, the proposed power clamp does not have snapback curve and has a low impedance during an ESD event. In addition, the structural characteristics of the proposed I/O clamp enable it to provide discharge paths for all four ESD discharge modes (PS, PD, NS, ND), and the clamp is more area efficient than conventional ESD protection circuits composed of gate-grounded n-type metal-oxide-silicon transistors or SCRs. Moreover, because floating regions are inserted in the I/O clamp and the clamp has a high holding voltage, the clamp design is resistant to latch-up, which is a critical drawback of snapback devices. Therefore, the proposed ESD protection circuit can effectively provide highly reliable protection to internal integrated circuits. The proposed circuit was fabricated using a 0.18 μm bipolar-CMOS-DMOS process, and the electrical properties and ESD robustness of the circuit were verified through a transmission line pulse measurement method and human body model surge application tests.**

Index Terms—**Electrostatic discharge(ESD), high current driving capability, lateral insulated gate bipolar transistor (LIGBT), silicon controlled rectifiers (SCR), holding voltage, ESD network**

I. INTRODUCTION

In the semiconductor industry, processes that require a continuous reduction in the size of integrated circuits (ICs) are being developed. Consequently, electrostatic discharge (ESD) has emerged as a major problem that affects the reliability of ICs [1, 2]. Particularly, with the decrease in the chip area, ESD-induced malfunction and breakdown in the normal state have been increasingly recognized as a serious problem [3, 4]. To solve this problem, ESD protection clamps such as gate-grounded n-type metal-oxide-silicon (GGNMOS) circuits and silicon-controlled rectifiers (SCRs) are commonly used. A GGNMOS circuit discharges ESD current through parasitic lateral NPN bipolar junction transistors (BJTs), is perfectly CMOS-compatible, and has excellent snapback range characteristics. However, because the current driving ability of a GGNMOS circuit is low, multi-fingers is used to improve its robustness; therefore, the GGNMOS circuit consumes a large area [5, 6]. Unlike a GGNMOS circuit, an SCR discharges ESD current through the positive feedback operation of parasitic lateral PNP and NPN BJTs, so it has excellent current driving ability and superior area efficiency. However, avalanche breakdown is induced between two well regions of the SCR, leading to a high trigger voltage. In addition, because of the high current gain of the parasitic BJTs, the holding voltage is low, which may cause the problem of latch-up [7, 8]. To address these

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problems of the SCR, various studies have aimed to improve its electrical properties. In addition, to verify the reliability of ESD protection between all the pins of the whole chip, four ESD test modes (PS, PD, NS, and ND) were developed for the tests between the input/output (I/O) pad and the V_{DD} or V_{SS} terminal and a test mode was developed for the test between the V_{DD} and V_{SS} terminals (DS) of the power line. The conventional GGNMOS and SCR circuits can ensure the reliability of the core IC by discharging the ESD current through the snapback operation of the lateral parasitic BJTs for the positive ESD current (PS, PD, and DS) flowing into the I/O pad or V_{DD} terminal. However, these conventional designs are highly vulnerable to negative ESD currents (NS and ND) because of the unidirectional characteristic of these designs. Thus, to achieve stable ESD discharge in the NS and ND modes, four ESD clamps are required, but this solution has the drawback of consumption of a very large space. Therefore, in this paper, a whole-chip all-directional ESD protection circuit is proposed. In this circuit, the conventional resistor-capacitor (RC)-based ESD detection circuit is used as the power clamp. In addition, a new I/O clamp structure is developed that is capable of responding to four ESD discharge modes at the I/O terminal. In the proposed circuit configuration, only two types of ESD clamps are required. Thus, the area efficiency is improved and a structural increase in the holding voltage is induced, thereby providing latch-up immunity.

II. Proposed Whole-Chip ESD Protection Circuit

1. ESD Protection Circuit based on Conventional ESD Clamp

Fig. 1 shows cross-sectional views of the conventional GGNMOS and SCR circuits. When a positive ESD current flows to the anode, the parasitic BJT begins to operate and causes snapback, and the ESD current is discharged at a low holding voltage. However, when a negative ESD current is introduced, it is discharged only through a PN diode in which a small perimeter is formed structurally, thus considerably reducing ESD reliability. Fig. 2 shows a whole-chip ESD protection circuit composed of a conventional ESD clamp and the I-V

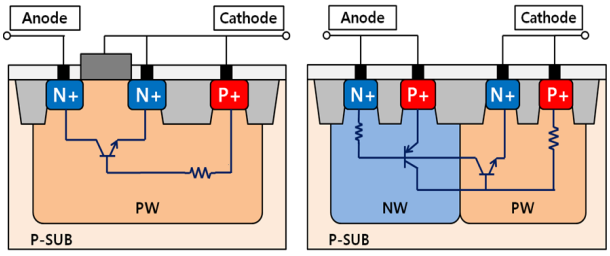


Fig. 1. Cross-sectional views of conventional GGNMOS (left) and SCR (right) ESD clamp structures.

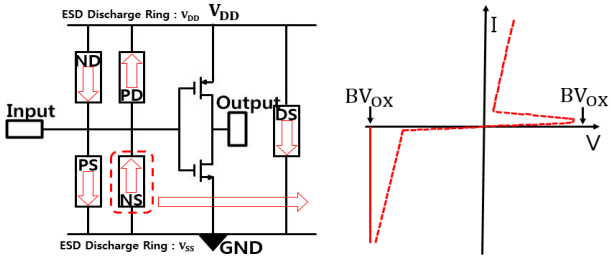
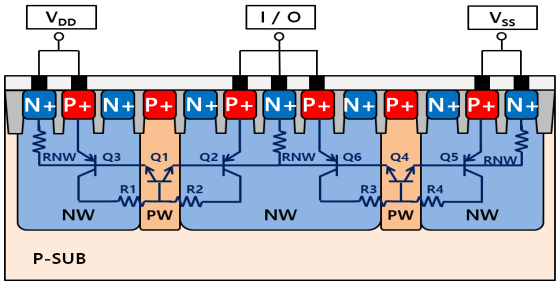


Fig. 2. ESD protection circuit composed of conventional snapback components and electrical properties of I/O clamp.

characteristics for each ESD discharge mode. Four ESD clamps (including the power clamp) are configured so that all the ESD discharge modes (PS, PD, NS, and ND) are considered. However, this circuit requires a considerably large area to achieve high ESD robustness.

2. Proposed All-directional ESD Protection Circuit and Its Operating Principle

Fig. 3 shows the cross-sectional view of the I/O ESD clamp of the proposed SCR-based ESD protection circuit and the equivalent circuit diagram including the ESD discharge paths. The proposed I/O clamp consists of six parasitic BJTs and eight parasitic resistors. The left part is connected to the V_{DD} terminal, the center part is connected to the I/O terminal, and the right part is connected to the V_{SS} terminal. The inserted floating regions increase the effective base lengths of the parasitic BJTs, reducing the emitter injection efficiency and increasing the holding voltage. The operating principle of the proposed I/O clamp in different modes is as follows. In the PD mode, when a positive ESD pulse flows to the I/O terminal, the potential of the N well rises and the left P well located in the direction of the V_{DD} terminal is reverse biased. When the electric field of the junction reaches the critical point, avalanche breakdown occurs and an electron-hole pair (EHP) is generated. The



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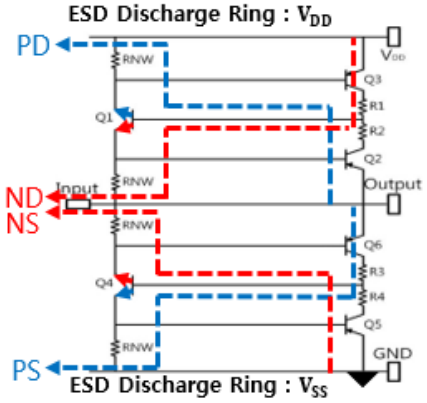


(b)

Fig. 3. (a) Cross-sectional view of proposed all-directional ESD protection structure, (b) its equivalent circuit (PD, ND, PS, and NS discharge paths).

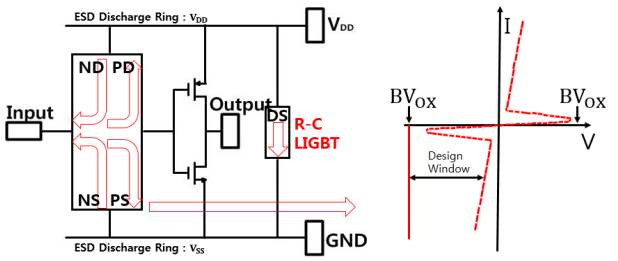


Fig. 4. Proposed ESD protection circuit and electrical properties of ESD clamp.

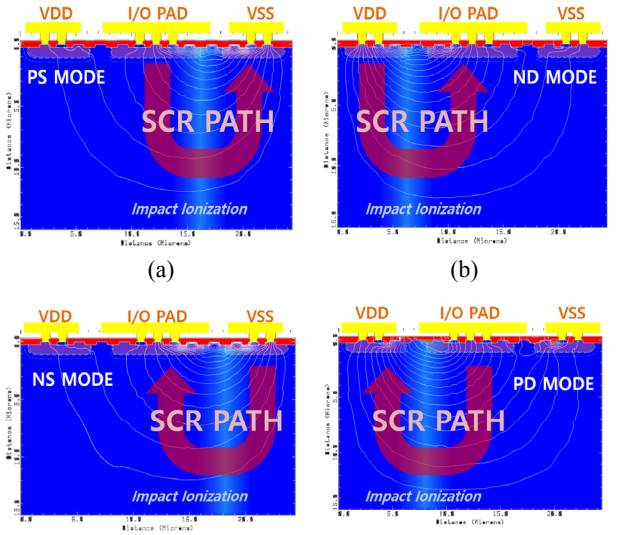


Fig. 5. Current path and impact ionization simulation results for I/O clamp of proposed I/O ESD Clamp (a) PS mode, (b) ND mode, (c) NS mode, (d) PD mode.

emitter-base junction of Q2 (PNP BJT) is forward biased by the generated EHP, and the current flowing through the turned-on Q2 (PNP) increases the potential of the P well, thereby turning on Q1 (NPN). The turned-on Q2 and Q1 supply a base current to each other to discharge the high ESD current through a latch operation. In addition, the effective base lengths of Q2 and Q1 increase because of the N+ and P+ floating regions, resulting in a high holding voltage.

The operating principle of the ND mode is the same as that of the PD mode, and a high ESD current is discharged by Q3 and Q1 this time. In addition, in the PS mode where a forward ESD surge is applied to the V_{SS} terminal, when a positive ESD pulse flows to the I/O terminal, the potential of the N well rises. When the electric field of the junction reaches the critical point, avalanche breakdown occurs, resulting in the generation of an EHP in the P well, and as previously described for the PD mode, the parasitic BJTs Q6 (PNP) and Q4 (NPN) are turned on. Through the latch operation of Q6 and Q4, a high ESD current is discharged, and in the case of the NS mode, an opposite path is formed. Therefore, although the proposed I/O clamp has a single structure (Fig. 4), its high holding voltage and double symmetrical structure enable it to provide appropriate responses to all four modes of the ESD discharge paths (PD, ND, PS, and NS) at the I/O pad. To demonstrate the operating mechanism of the proposed I/O clamp, a lateral current path simulation was performed using a two-dimensional technology computer-aided design tool. To examine the operating principle of the device under ESD stress, a human body model (HBM)-based 4 kV ESD surge formed in a 100 pf capacitor and a 1.5 kΩ resistor was applied to the proposed structure through mixed-mode simulation [9, 10]. Fig. 5 presents the simulation results, which show the lateral current flow with impact ionization line. In all the four modes, leakage current transport due to the reverse junction potential was observed before the trigger, and finally, parasitic SCR

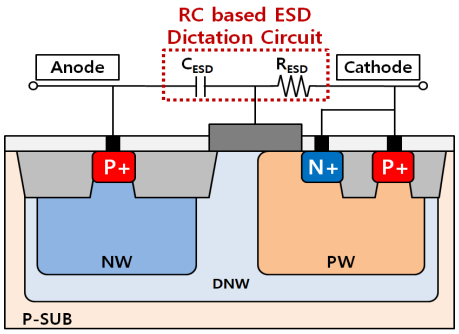


Fig. 6. Cross-sectional view of R-C LIGBT structure and layout (DS).

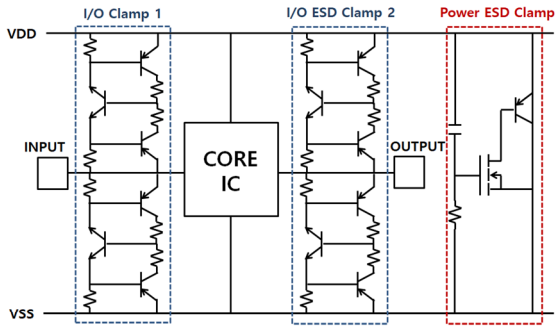


Fig. 7. Full equivalent circuit diagram of proposed all-directional ESD protection circuit with I/O and power clamps.

paths of the same type with a uniform current flow running deep into the substrate were observed.

Fig. 6 shows a cross-sectional view of a power ESD clamp applied to the proposed ESD protection circuit. Power clamps generally require a higher operating voltage than I/O clamps. To achieve a flexible response to the latchup phenomenon caused by the load resistance of the I/O clamp, the power ESD clamp was composed of an ESD detection circuit with an RC circuit and a lateral insulated-gate bipolar transistor (LIGBT) with a relatively high current density. When an ESD surge with a high frequency characteristic is applied to the anode, a bias is applied to the gate terminal of the LIGBT, and the residual ESD current is discharged through the operation of the LIGBT. Hence, the power clamp of the proposed ESD protection circuit is relatively free from latchup and allows the optimization of the I/O clamp for the required ESD design window by appropriately adjusting the values of resistors and capacitors according to the V_{DD} value of the core IC. Fig. 7 shows the equivalent circuit diagram of the proposed ESD protection circuit with I/O and power clamps. The proposed ESD protection circuit

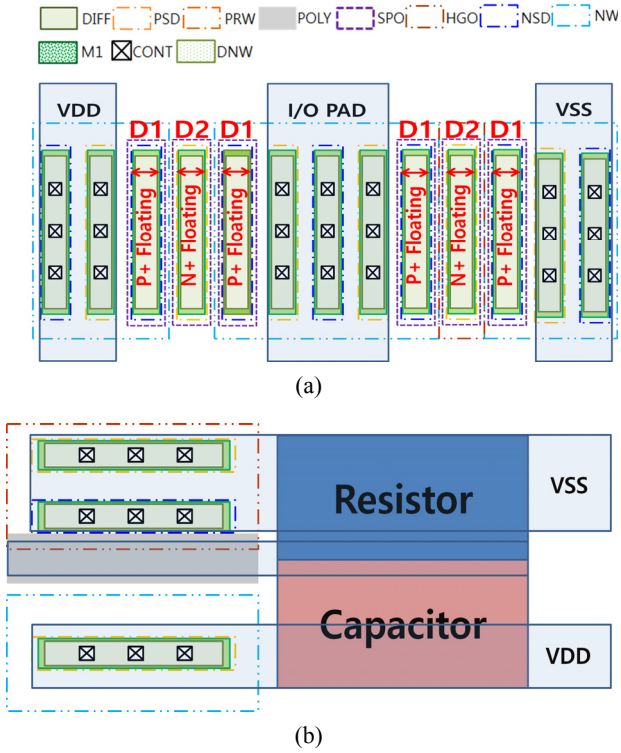


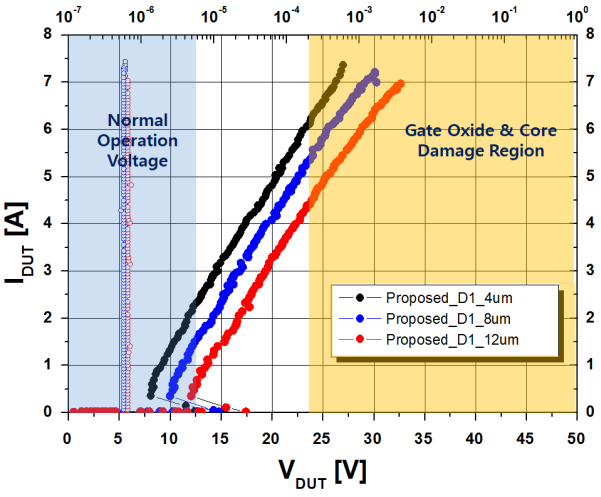
Fig. 8. Layout of proposed ESD protection circuit components (a) I/O clamp, (b) power clamp.

has only one I/O clamp, which is applied to each of the input and output terminals, thereby achieving superior area efficiency compared to the conventional ESD protection circuit, which includes four I/O clamps (one for each terminal).

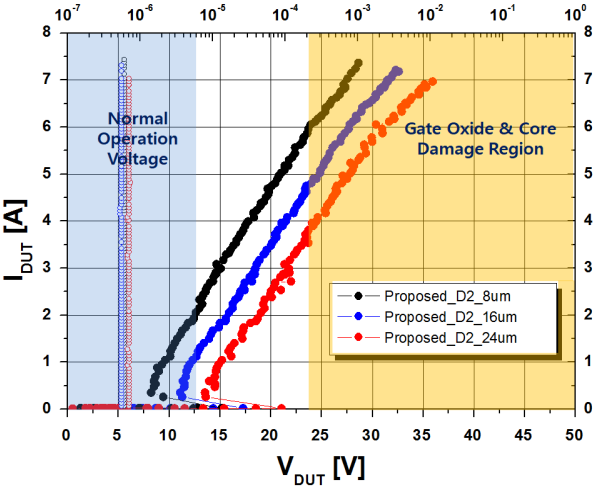
III. Measurement Results and Discussion

1. Optimization of Electrical Properties

The proposed ESD protection circuit and conventional ESD clamps were fabricated through a 0.18 μm CMOS process and were optimized for application at 12 V considering the drain-to-source breakdown voltage (BVDSS) and oxide breakdown voltage (BVox) of the process. The 12 V ESD design window of the 0.18 μm CMOS process was formed between 13.2 V (operation voltage + safe margin of 10%) and 24 V (oxide breakdown voltage) [11]. To verify the electrical properties of the proposed ESD protection circuit, a transmission line pulse (TLP) measurement method with a rising time of 10 ns and a pulse width of 100 ns was used [12]. The measurement results obtained from the



(a)



(b)

Fig. 9. Variation in holding voltage according to changes in design variables (a) D1, (b) D2.

TLP system are illustrated as an I-V curve, and the key parameters of the snapback device (Vt1, Vh, and It2) are presented. Fig. 8 shows the layout of the I/O and power clamps of the proposed ESD protection circuit and the associated design variables. Each floating region of the I/O clamp was selected as the design parameter. The design variable D1 represents the P+ floating region, and as D1 increased, the lengths of the base regions of the NPN parasitic BJTs (Q1 and Q4) increased and the emitter injection efficiency reduced. On the other hand, D2 represents an N+ floating region, and an increase in D2 decreased the emitter injection efficiency of the PNP parasitic BJTs (Q2, Q3, Q5, and Q6) and increased the holding voltage. Fig. 9(a) shows that the holding voltage

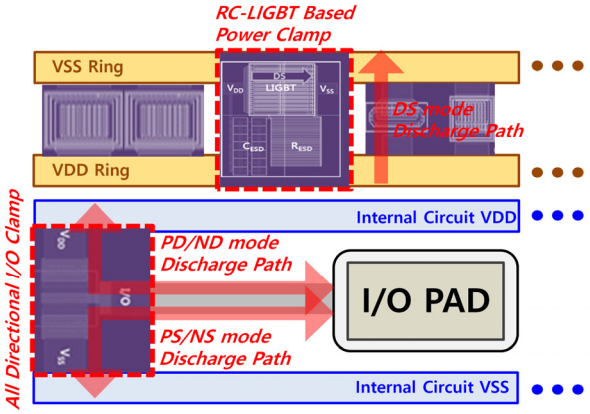
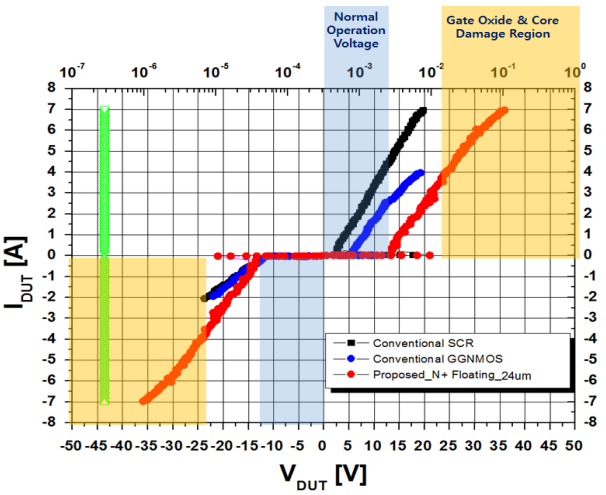


Fig. 10. Configuration of whole-chip ESD protection circuit.

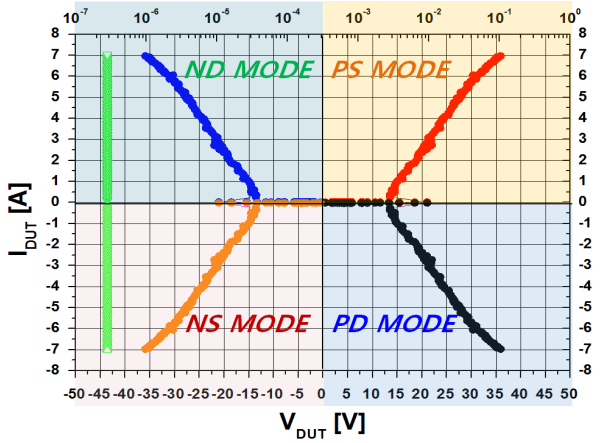
increased to 12.4 V as D1 changed from 4 μm to 12 μm, and Fig. 9(b) shows that the holding voltage of the I/O clamp increased up to 13.1 V as D2 increased from 8 μm to 24 μm. In this experiment, the area increase induced by the design variable D2 was half of that induced by D1. Hence, the length for D2 was doubled for the same increase in the area. According to the measurement results, in the case of the NPN parasitic BJTs (Q1 and Q4), the design variable D2 allowed more effective control of the holding voltage than D1 because the same feedback loop was formed in both the forward and reverse modes. Therefore, the proposed I/O clamp was optimized for the 12 V ESD design window by adjusting the design variable D2.

2. Comparison between Electrical Properties of Optimized I/O Clamp and Conventional ESD Clamps

Fig. 10 shows the configuration of the whole-chip ESD protection circuit according to the components and ESD discharge paths. Fig. 11(a) shows the TLP measurement results for the optimized I/O clamp (D2 = 24 μm) and the conventional ESD protection devices. The proposed structure and the conventional GGNMOS and SCR circuits were all fabricated through a 0.18 μm bipolar-CMOS-DMOS (BCD) process, and all the devices had the same width to achieve proper comparison of their electrical properties. The area of the proposed I/O clamp is 9796um^2(124 um * 79 um), which is much larger compared to the conventional GGNMOS (33 um * 79 um = 2607 um^2) and SCR (39 * 79 = 3081 um^2). However, GGNMOS needs to increase the number of multi-fingers to achieve improved It2, and SCR needs



(a)



(b)

Fig. 11. (a) TLP measurement results for proposed I/O clamp and conventional GGNMOS and SCR circuits (PS and NS), (b) TLP waveforms for four ESD modes of proposed I/O clamp (PD, ND, PS, and NS).

to increase the implant spacing to optimize the ESD Design Window. Also, since the two traditional structures only operate in positive ESD mode, they must be configured with four clamps to account for the polarity of the ESD surge. On the other hand, the proposed structure has excellent area efficiency as it can respond to ESD surges in all modes with one clamp. According to the measurement result, the holding voltages of the conventional GGNMOS and SCR circuits were 6.2 and 2.6 V, respectively. In comparison, the proposed I/O clamp had a high holding voltage of 13.3 V owing to a large decrease in the emitter injection efficiency, which was achieved by inserting floating regions and optimizing the length variation. This voltage value was

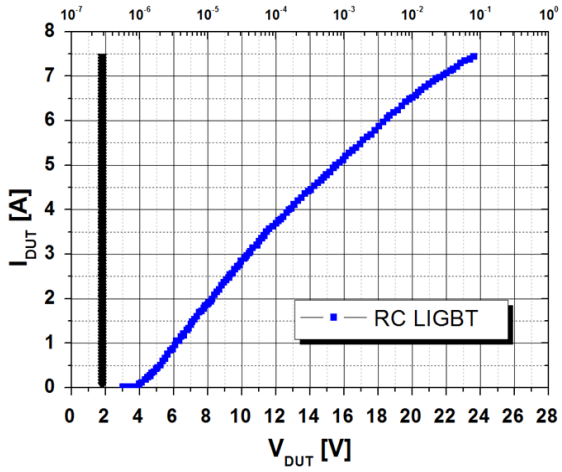


Fig. 12. TLP measurement results for RC LIGBT-based power clamp.

adequate for the 12 V ESD design window. In addition, unlike the conventional GGNMOS and SCR circuits in which different diode operation characteristics were observed in the reverse mode, the proposed I/O clamp exhibited the same waveform in the reverse mode as well. Fig. 11(b) shows the TLP measurement results for the proposed I/O clamp in four modes while considering the ESD polarities of the I/O pad, VDD terminal, and VSS terminal. Because the proposed I/O clamp had a double-symmetrical structure, in all the four ESD modes, snapback was induced because of the formation of internal SCR paths and a high secondary breakdown current (It2) was achieved at 7 A. Fig. 12 shows the TLP waveform for the power clamp of the proposed ESD protection circuit. When an ESD event occurred at the VDD terminal, the voltage corresponding to the gate region of the LIGBT increased because of the ESD detection circuit, and the transient gate bias of the LIGBT device exceeded the critical voltage in the turned-on state with a low channel resistance. In addition, the reverse breakdown voltage of the LIGBT was 20 V and It2 was 7.4 A. Table 1 lists the main electrical properties of all the fabricated ESD clamp structures.

3. Results of High-temperature Reliability Test

The thermal reliability of the proposed ESD protection circuit at high temperatures (300-500 K) was determined (Fig. 13 and 14) [13, 14]. In the thermal reliability test, the wafer was heated using a hot-chuck control system,

Table 1. Summary of the electrical characteristics of all fabricated structures

Structure		Operation Mechanism	Trigger Voltage (Vt1)	Holding Voltage (Vh)	Holding Current (Ih)	2nd Breakdown Current (It2)	Area
Conventional Clamp	GGNMOS (PS Mode)	Snapback	9.7	6.2 V	0.26 A	3.91 A	2607 um^2
	SCR (PS Mode)	Snapback	17.5 V	2.6 V	0.34 A	6.96 A	3081 um^2
Proposed I/O Clamp	PS Mode	Snapback	20.9 V	13.3 V	0.37 A	7.02 A	9796 um^2
	NS Mode	Snapback	20.3 V	13.1 V	0.33 A	6.99 A	
	PD Mode	Snapback	20.7 V	13.4 V	0.34 A	6.97 A	
	ND Mode	Snapback	20.5 V	13.3 V	0.38 A	7.01 A	
Proposed Power Clamp	DS Mode	Non-Snapback	Vt = 4.02 V			7.5 A	12507 um^2

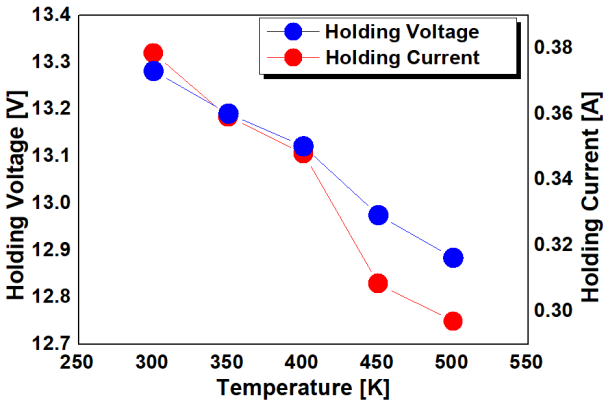


Fig. 13. Holding voltage and current characteristic results obtained for high temperatures (300-500 K).

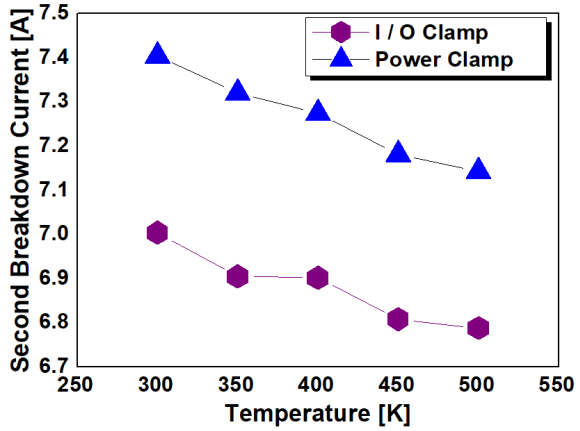


Fig. 14. Second breakdown current characteristic results obtained for high temperatures (300-500 K).

and the electrical properties were evaluated through TLP system measurements.

The high-temperature characteristics are important because they affect the electrical properties and It2 of the ESD protection circuit. As the temperature increased, the carrier mobility decreased, thereby increasing the parasitic resistance of the well region and causing a decrease in the clamping range and heat loss of It2. According to the measurement results, at a high temperature of 500 K, the proposed I/O clamp had a holding voltage of 12.9 V, holding current of 298 mA, and secondary trigger current of 6.98 A. In addition, the power clamp had a secondary trigger current of 7.1 A. The holding voltage of the I/O clamp of the proposed ESD protection circuit was still higher than 12 V, which is the normal operating voltage of the internal circuit, and both the I/O and power clamps had secondary trigger currents of 6.5 A or higher, indicating the excellent ESD robustness of the proposed circuit for an HBM above 6 kV (calculated as (1500 + Ron) × It2). Therefore, the proposed ESD protection circuit has excellent thermal reliability and high-temperature characteristics.

IV. Conclusion

In this paper, we propose a design for a whole-chip all-directional ESD protection circuit. The proposed ESD protection circuit consists of only two types of ESD clamps: an I/O clamp and a power clamp. The I/O clamp provides discharge paths with a high holding voltage for each ESD stress mode (PD, ND, PS, and NS) that can occur at the I/O pad, V_{DD} terminal, and V_{SS} terminal. The proposed I/O clamp was optimized for the 12 V I/O ESD design window by specifying the lengths of the inserted floating regions as a design variable and analyzing the electrical properties. In addition, the RC LIGBT-based ESD protection circuit provides a discharge path for the V_{DD}-to-V_{SS} mode (DS) and exhibits latchup immunity with regard to the supply clamp voltage. The proposed

whole-chip all-directional ESD protection circuit was fabricated using a 0.18 μm BCD process, and its electrical properties were examined through TLP system measurements. In addition, a hot-chuck controller was used to investigate changes in the electrical properties at high temperatures. The proposed all-directional ESD protection circuit shows excellent robustness for an HBM above 6 kV at a high temperature of 500 K. Therefore, it is expected that the proposed circuit can be employed for 12 V applications, can provide good area efficiency, and can enhance the reliability of the core IC.

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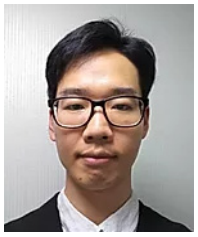

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