High-PSRR Low-dropout Regulator with Fast Transient Response Time and Low Output Peak Voltage

Nahyun Kim and Junyoung Song

Abstract—This study proposes the feed-forward ripple cancellation (FFRC) technique to low drop-out (LDO) regulator. By adding load tracking impedance to the gate of pass transistor, it is possible to secure stability with a 100-nF capacitor having low ESR and be obtained less than 35 ns response time. In all frequency bands, a power supply rejection ratio (PSRR) less than -70 dB is obtained when the load current is 10 mA. The circuit is implemented in 65-nm CMOS process.

Index Terms—Low-dropout (LDO) regulator, power-supply rejection ratio (PSRR), fast transient response time, low output peak voltage

I. INTRODUCTION

Analog applications and the device that deal with small signals continue to become smaller and more functional as the modern technology advance. Therefore, a LDO should provide the system with clean and ripple-free power because a voltage ripple can cause a fatal defect in the noise-sensitive RF/analog blocks. There are two reasons why the LDO supply voltage change: i) line regulation by input voltage swing; ii) load transient response by load current rapid change.

Fig. 1 explains the line regulation and the load transient response. The line regulation is the ability to supply a less variable output voltage \( V_{\text{LDO\_OUT}} \) despite of changes in the input voltage \( V_{\text{LDO\_IN}} \). The LDO regulator with a lower PSRR (i.e., \( 20\log\left( \frac{V_{\text{LDO\_OUT}}}{V_{\text{LDO\_IN}}} \right) \)) is not efficient [1]. The load transient response refers to how much the output voltage \( V_{\text{LDO\_OUT}} \) fluctuates when the step of load current \( I_{\text{LDO\_OUT}} \) is present. The output transient response should not deviate significantly from the regulated value and should be promptly restored to a target voltage. As the output capacitor \( C_{\text{OUT}} \) increases, the transient response time also increases [2]. When \( C_{\text{OUT}} \) is reduced to achieve fast transient time, the equivalent-series-resistance \( R_{\text{ESR}} \) had to be large because stability must be ensured using pole-zero cancellation (i.e., \( Z_{\text{ESR}}=1/C_{\text{OUT}}R_{\text{ESR}} \)) [3]. A high \( R_{\text{ESR}} \) degrades the performance of a load transient response while inducing a high voltage spike [2].

In [4], fast transient response is obtained by adaptively biased error amplifier, however, the voltage spike is large. In [5], the overshoot is reduced, but PSR is still low. The circuit in [6] achieves a -56 dB PSRR, but the load transient performance is not good because \( R_{\text{ESR}} \) is as large as 30-mΩ. Moreover, in previously introduced circuits in [7-9] with fast load transients, they show poor
PSRR performance.

The output ripple by input ripple is suppressed using FFRC technique [6]. In this paper, the structure is simpler than [6] by eliminating the summing amplifier that merges the feedback regulating loop with feed-forward path at the gate of the pass transistor. And, the non-dominant pole is moved behind the unity-gain frequency (UGF) by adding a load-tracking impedance at the gate of pass-transistor. Therefore, a stability is guaranteed while reducing both the transient response time and the output spike. The proposed LDO supplies a low-ripple and stable signal with little change even if the input voltage and output current are changed. Section II discusses the structure and the implementation of circuit. The simulation results and performance comparison are shown in Section III. Finally, the conclusions are provided in section IV.

II. PROPOSED LDO ARCHITECTURE AND CIRCUIT IMPLEMENTATION

Fig. 2 presents the proposed LDO regulator. The proposed LDO applies a load-tracking impedance adjustment and loop-gain boosting technique with a feed-forward amplifier [6, 7]. In Fig. 2, $M_{PT}$ is the pass transistor and $M_{c1}$, $M_{b4}$, $M_{i0}$ and $M_{i0}$ constitute the folded common-gate amplifier. Similar to the design reported in [8], $M_{b1}$, $M_{b2}$ and $M_{b1}$ - $M_{b5}$ constitute a control voltage (i.e., $V_{CTRL}$) generator for the gate voltage of $M_{c1}$. The reference voltage $V_{REF}$ (e.g., bandgap voltage reference), $R_{b}$ and $M_{b0}$ provide the bias current, and $C_{g}$ is a filtering capacitor.

$C_{OUT}$ and $R_{ESR}$ are reduced to improve load transient performance. Since this architecture has a 100-nF output capacitor which has low $R_{ESR}$, the $Z_{ESR}$ is located after the UGF which is about 10-MHz. Therefore, $p_1$ generated by the gate of $M_{PT}$ must also be located beyond the UGF, and only $p_1$ (i.e., $|C_{OUT}[(r_{c,PT} || g_{m,c1})]|^{-1}$) must locate before the UGF. By reducing the resistance of the gate using diode-connected $M_{b5}$, $p_2$ is also pushed back to 10-MHz. Even if the output current ($I_{OUT}$) and UGF increase, $g_{m,b5}$ and $p_2$ also increase and the stability is ensured. $M_{b3}$ and $M_{b4}$ boost the gain that fell due to the load-tracking impedance. The poles at $\gamma_1$, $\gamma_2$ must also be located beyond the UGF. The pole at $\gamma_1$ is located at 107 MHz because $C_{g,b1} = 1.7 \text{ fF}$, $r_{c,b1} = 1.64 \text{ M}\Omega$ and $r_{c,b4} = 1.84 \text{ M}\Omega$. The pole at $\gamma_2$ is located at 369 MHz because $C_{g,b4} = 362 \text{ aF}$, $r_{c,b1} = 3.2 \text{ M}\Omega$, and $r_{c,b2} = 1.89 \text{ M}\Omega$. Fig. 4 depicts the simulated loop gain-phase plot under different $I_{OUT}$ ranging from 2 mA to 10 mA. The phase margin is higher than 60°.

With a mathematical model of the LDO shown in Fig. 3, the transfer gain from input to output is obtained as below.

\[
\frac{V_{OUT}(s)}{V_{IN}} = \frac{1 + g_{m,REF}r_{d,REF} \left[ 1 + PSRR, g_{n,05}, R_{pout}, H_{x}(s) \right]}{1 + \frac{r_{d,REF}}{Z_L(s)} + g_{m,REF}r_{d,REF}, A_1, A_2, g_{m,04}, R_{pout}}
\]

……. (1)
where $PSRR_e$, $A_C$, $A_e$ and $R_{gav}$ are the power-supply rejection ratio of the error amplifier, $g_{m,1}(r_{a,1} \parallel r_{a,4})$, $g_{m,01}(r_{a,01} \parallel r_{a,02})$ and $(r_{a,03} \parallel r_{a,04}) g_{m,05}^{-1}$, respectively.

From Eq. (1), an optimal $H_g(s)$ is figured out to prevent the output ripple for the input ripple. That is, the LDO transfer function must be zero for the enhanced PSRR [6].

$$H_g(s)_{|_{opt}} = -\left(\frac{PSRR + \frac{1}{g_{m,MFF} r_{a,MFF}} + 1}{g_{m,03}(r_{a,03} \parallel r_{a,04} \parallel g_{m,05})}\right)$$

(2)

The PSRR greatly improves when the gain of the feed-forward amplifier is as shown in Eq. (2). The improvements will be introduced in the next section.

III. SIMULATION RESULTS

Fig. 5 presents the simulated load transient responses of the proposed LDO regulator. The output voltage when $I_{OCT}$ is switched from 2 mA to 10 mA with 10 ns rise/fall times ($\Delta t$) is simulated. As a result, the undershoot/overshoot are less than 861 $\mu$V and the response time is less than 35 ns.

Fig. 6 shows a comparison of the PSRR simulation results based on the presence or absence of FFRC. The PSRR is worse than 42-dB without feed-forward amplifier. By adding a feed-forward amplifier and removing the output ripple, 91-dB PSRR in DC and 70-dB PSRR at 46 MHz are obtained. After 46 MHz, the PSRR is improved again by the effect of $C_{OCT}$ [1].

The performance summary and comparison is shown in Table 1. The proposed LDO is sufficiently stabilized with a 100-nF output capacitor while [6, 13] use a capacitor over 1 F. $I_0$ is not large when compared with others. The response time is 35 ns, which is the fastest compared to other structures. Finally, the proposed LDO regulator has an improved PSRR of -91 dB.

IV. CONCLUSIONS

The proposed LDO regulator includes a feed-forward amplifier and a load tracking impedance. By applying the proposed idea, an improved PSRR and a low output peak voltage are achieved with 100-nF output capacitor which has low-ESR. Finally, this design provides a stable voltage quickly even if the input voltage and output current change.
Table 1. Performance summary

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<tr>
<td>V_m (V)</td>
<td>130</td>
<td>350</td>
<td>180</td>
<td>350</td>
<td>65</td>
<td>40</td>
<td>65</td>
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<td>V_acc (V)</td>
<td>&gt; 1.15</td>
<td>1.5-3</td>
<td>1.35</td>
<td>5</td>
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<td>1.1-1.9</td>
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<td>V_m (V)</td>
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<td>0.3-1.8</td>
<td>0.15</td>
<td>3.2</td>
<td>0.04-0.24</td>
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<td>I_o (μ A)</td>
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<td>26</td>
<td>15</td>
<td>N/A</td>
<td>116-874</td>
<td>56</td>
<td>27</td>
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<td>C_acc(μ F)</td>
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<td>0.1</td>
<td>0.22</td>
<td>N/A</td>
<td>Cap-free</td>
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<td>0.1</td>
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<td>R_acc (mΩ)</td>
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<td>23</td>
<td>1000</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>T (μ s)</td>
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<td>N/A</td>
<td>4.92</td>
<td>0.077</td>
<td>N/A</td>
<td>0.035</td>
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<td>PSRR (dB)</td>
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<td>-67@1MHz</td>
<td>N/A</td>
<td>&gt; -18</td>
<td>&gt; -67.26</td>
<td>-18@100k</td>
<td>-10@1MHz</td>
</tr>
<tr>
<td>@ Freq (Hz)</td>
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<td>-67@1MHz</td>
<td>N/A</td>
<td>&gt; -18</td>
<td>&gt; -67.26</td>
<td>-18@100k</td>
<td>-10@1MHz</td>
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<tr>
<td>ΔV_ac /V_acc</td>
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<td>56 m</td>
<td>5.2 m</td>
<td>5.96 m</td>
<td>80 m-137 m</td>
<td>140 m</td>
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<td>rise/fall times</td>
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<td>N/A</td>
<td>900 ns</td>
<td>10 ns</td>
<td></td>
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*Measured value

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REFERENCES


[12] M. A. Akram, W. Hong, I.-C. Hwang,


Nahyun Kim was born in Incheon, Korea, in 1998. She will receive the B.S degree in electronic engineering from the Incheon National University, Korea, in 2022. She has been working on analog design including power management circuit. Ms. Kim received the Excellence Award at the result presentation of the “Advanced Course for Women’s Graduate School Student Engineering Research Team” under the theme of "Low-Power Decision Feedback Equalizer for 28Gb/s Interface in 65nm CMOS Process" in 2020.

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