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Demonstration of Multi-layered Macaroni Filler for Back-Biasing-Assisted Erasing Configuration in 3D V-NAND

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Abstract—**Controlling the erase speed of a NAND flash is one of the challenges in memory technology. As the planar NAND flash has evolved to the vertically integrated gate-all-around (GAA), the number of stacks of word-lines (WL) was increased for better packing density. However, potential transfer through the silicon substrate or metal bit-line (BL) is insufficient with the increased number of stacks. Hence, we propose a novel V-NAND structure including multi-layered macaroni filler. The proposed macaroni filler is composed of a dielectric outer layer and a metallic core layer. The metallic core layer makes back-biasing is possible in V-NAND. As a result, erase speed can be improved without large modification of fabrication process or device layout.**

Index Terms—**Back-biasing, data erase, flash memory, macaroni filler, 3-dimensional (3D) V-NAND**

I. INTRODUCTION

As the pandemic accelerates the untact era, demand for mobile electronics has rapidly increased. Especially, NAND flash storage, which consists of memory cells, enables storage of data semi-permanently. Typically, memory cells contain a charge trap layer (CTL) composed of Si_3N_4, as gate dielectric. The device structure of the cells in NAND flash has evolved from 2-dimensional (2D) to 3-dimensional vertical NAND (V-NAND) for better density and lower bit-cost.

In this context, recently, most NAND flash storage is fabricated based on the V-NAND structure [1-3]. Compared with the 2D based memory cell, V-NAND includes a poly-silicon channel, as well as a buried dielectric layer underneath the channel. The buried dielectric is called a macaroni oxide filler because of its geometry; it reduces variability stemming from poly-silicon grains [4]. For this reason, in contrast to back-biasing as applicable in 2D based memory cells for better erase speed and operating configuration, back-biasing in V-NAND is impossible due to the existence of the macaroni filler. Typically, there are several ways to improve erase speed of V-NAND.

The first approach is gate dielectric engineering. For example, bandgap engineering of tunneling oxide (*e.g.*, BE-ONO) has already been applied for mass production [5, 6]. However, even though high-*k* dielectrics such as Al_2O_3 have been applied [7], further improvement of erase speed by gate dielectric engineering is difficult due to uncontrollable gate leakage. The second approach is to use a novel erase configuration such as thermal erase [8, 9]. The operation principle of the thermal erase is based on thermal excitation of electrons under an intentionally-created high temperature environment. However, application of thermal erase is difficult due to its complex operating configuration, high power consumption, and thermal disturbance among memory cells.

The third approach involves bias configuration. For

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example, gate-indented-drain-leakage (GIDL), a phenomenon in semiconductor physics, can be intentionally triggered [10]. When high drain-to-gate bias (V_{DG}) is applied. Then, excessive holes are generated and drift from the drain to source through the poly-silicon channel. The holes increase the channel potential and induce back-biasing in V-NAND. However, unfortunately, as the number of V-NAND layers increases, the resistance of poly-silicon also increases. Hence, control of hole injection and drift is difficult to improve. Although J. Jang *et al.*, [2] at Samsung Electronics Inc. demonstrated that back-biasing is available in TCATs (Terabit Cell Array Transistor), back-biasing through a silicon substrate is only applicable for cells in lower stories.

In this paper, we propose a novel V-NAND structure and fabrication process. Multi-layered macaroni fillers composed of metallic core layers and dielectric outer layers are proposed to maximize V-NAND erase speed. Through the metallic core layer, back-biasing potential can be effectively transferred to all cells along the bit-line (BL) direction. The back-biasing of gate-all-around (GAA) memory cells can improve erase efficiency. All of the fabrication process and layout are compatible with the standard V-NAND process. A comparison between the conventional V-NAND and the proposed structure will be carried out under 3D simulations.

II. EXPERIMENTAL DETAILS

Fig. 1 shows the fabrication process flow of the proposed V-NAND structure for back-biasing. SiO_2 and Si_3N_4 are deposited iteratively on an Si-substrate, as shown in Fig. 1(a). After dry etching (Fig. 1(b)), O/N/O layers and a-Si (poly-Si) are deposited on the sidewall. The O/N/O can be modified into BE-ONO, but no such layer was included in our simulation.

Then, barrier SiO_2, which plays a role in isolation, is deposited underneath the poly-silicon channel. An electrical conductive metallic (or metal) core layer fills the trench, as shown in Fig. 1(c). Unlike conventional V-NAND strings that include macaroni fillers composed of only SiO_2, our proposed structure has a multi-layered macaroni filler composed of a metallic core layer and barrier SiO_2 [11]. After that, etching of the top side and heavy doping of poly-Si deposition are performed for

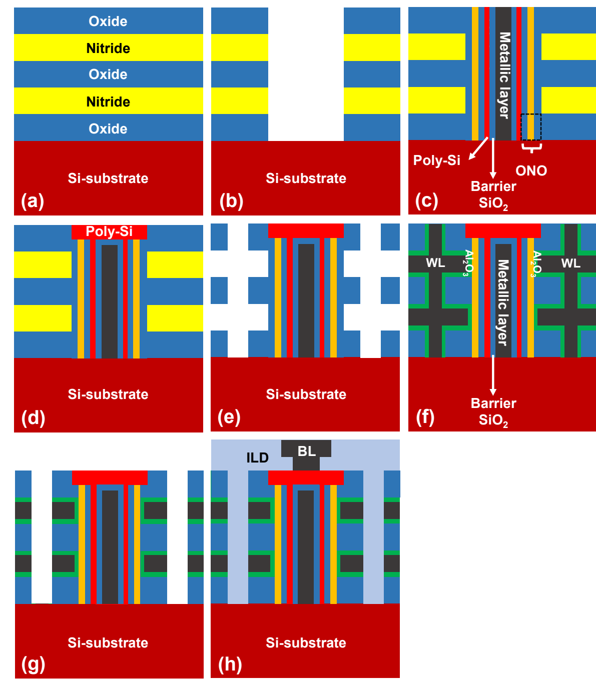

Fig. 1. Fabrication process flow of V-NAND containing multi-layered macaroni filler (a) and (b) Deposition of oxide and sacrificial silicon nitride layer, and dry etching of hole, (c) Deposition of dielectric layers, poly-silicon channel, barrier oxide isolation, and electrical conductive metallic core layer, (d) Etching of top layers and deposition of oxide to avoid electrical short between BL and metallic core layer. Then, heavily doped poly-silicon deposition for bit-line definition, (e) Selective etching of sacrificial silicon nitride and oxide layer, (f) Deposition of blocking oxide such as Al_2O_3 and WL metal, (g) and (h) Node separation, inter layer dielectric (ILD) deposition, and BL metallization.

drain region definition, as shown in Fig. 1(d). Then, dry etching, sacrificial Si_3N_4 removal, high-k blocking oxide deposition, and word-line (WL) formation are performed (Fig. 1(e)-(g)). Finally, node separation and BL formation are performed (Fig. 1(g) and (h)).

The proposed fabrication processing and applied materials are fully compatible with current NAND fabrication processing. Simulation studies to observe voltage distribution through the metallic core layer were performed by aid of the 3D simulator COMSOL. There are two reasons why we have used COMSOL as a simulator.

The first reason is for better simulation speed. Device structure in our proposed structure is very complex as well as contains a lot of boundary conditions. Therefore, the COMSOL can be preferred when using semiconductor models are not required. Considering, this work focuses on voltage distribution through the metallic

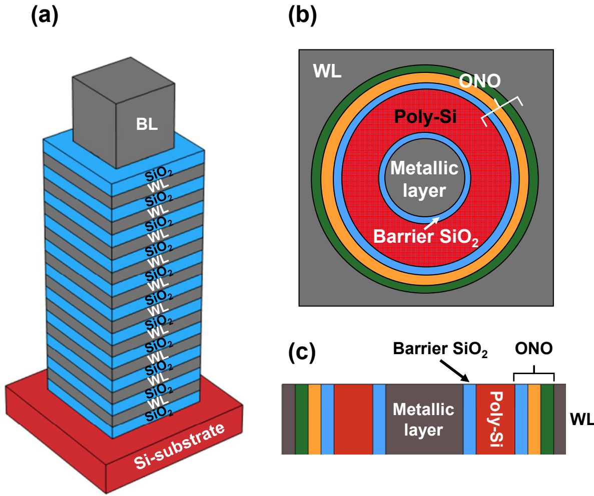

Fig. 2. (a) Tilted-view of proposed V-NAND string, (b) Cross-sectional image of the proposed structure cut along the WL, (c) Cross-sectional image of the proposed V-NAND cut along the BL.

layer, applying semiconductor simulator which requires lots of calculations are ineffective. The second reason is for fair comparison with our previous work [11]. Even though we have inferred that it is possible to apply back-biasing through the metallic core layer, the evidence was not enough. In this context, we performed simulations under the identical test vehicles such as simulator (*i.e.*, COMSOL), back-bone structure, and materials. It was also confirmed that potential distribution extracted by COMSOL, was well matched with the measured data [12].

Fig. 2(a) shows the schematic geometry of the proposed V-NAND string for simulation. A V-NAND string was designed with 10th floored WL for better simulation environment. Fig. 2(b) and (c) show cross-sectional view of the proposed NAND string cut along the WL and BL directions. Compared to conventional V-NAND, the proposed V-NAND includes a metallic core layer surrounded by barrier SiO_2 and poly-silicon channel (Fig. 2(b)). Considering process compatibility with conventional fabrication processing, the metallic layer was assumed to be identical to the WL material. Moreover, considering that the electrical conductivity of thin film tungsten is lower than that of bulk of 1.8×10^7 S/m, the value was assumed to be 10^7 S/m [13]. Other device geometry information was taken from previous papers [11, 14, 15]. Detailed device dimensions and material information used for simulation are summarized in Table 1.

Table 1. Parameters for simulation of multi-layered macaroni filler

	Dimension [nm]	Material
WL thickness	20	W
Channel thickness	25	Poly-Si
Metallic core layer diameter	21	W
Barrier oxide thickness	4	SiO_2
Tunneling oxide thickness	5	SiO_2
Nitride thickness	8	Si_3N_4
Blocking oxide thickness	10	Al_2O_3
Si-substrate thickness	50	Si
BL thickness	100	W
Inter layer dielectric thickness	20	SiO_2

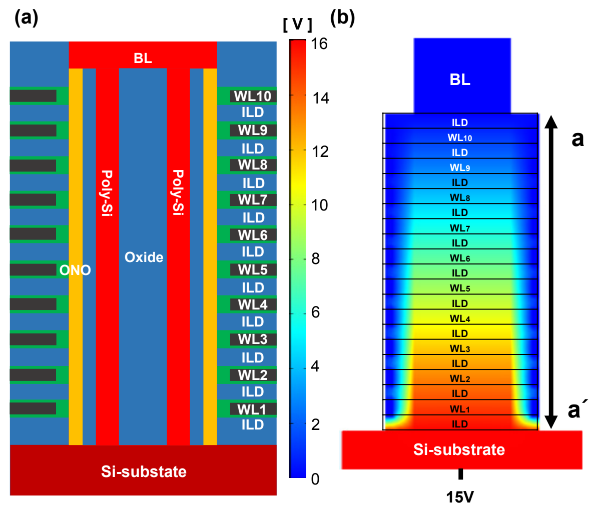

Fig. 3. (a) Cross-sectional schematic of conventional V-NAND flash string along BL direction, (b) Cross-sectional simulated potential distribution when positive voltage (15 V) is applied to silicon substrate.

III. Results and Discussion

Fig. 3(a) shows a cross-sectional schematic image of a conventional V-NAND string. When back-bias of 15 V is applied through the bottom silicon substrate, the voltage is gradually distributed along the BL direction because of the low electrical conductivity of the macaroni oxide and poly-silicon channel (Fig. 3(b)). The voltage distribution along the BL is not uniform; hence, the conventional V-NAND structure is not suitable for back-biasing-assisted erase configuration.

Fig. 4(a) shows a cross-sectional schematic image of the proposed V-NAND string. In contrast to the conventional V-NAND, proposed structure includes multi-layered macaroni filler composed of metallic core

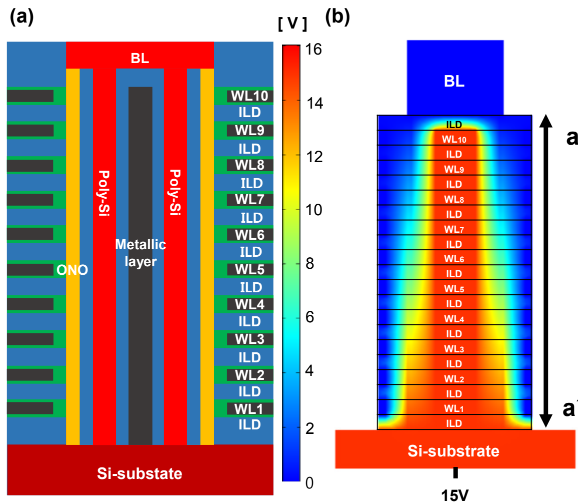

Fig. 4. (a) Cross-sectional schematic of proposed V-NAND flash string along BL direction, (b) Cross-sectional simulated potential distribution when positive voltage (15 V) is applied to silicon substrate.

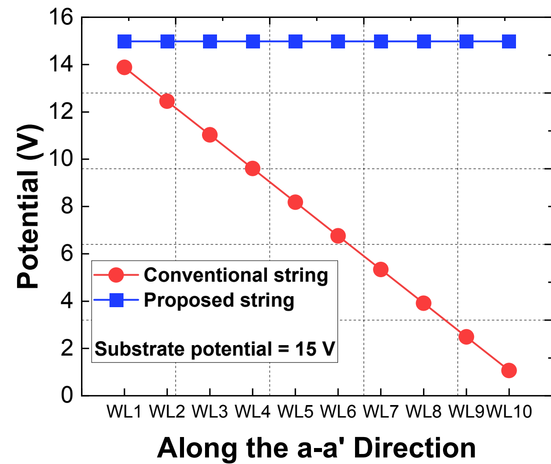

Fig. 5. Potential distribution extracted from Fig. 3 and 4. The potential of the proposed structure was extracted at the surface of the metallic core layer. In the conventional structure, identical point with the proposed structure was extracted for the fair comparison.

layer and the dielectric outer layer such as SiO_2. There is no structural difference between the conventional and the proposed V-NAND structure except for metallic core layer. It has already been reported that the metallic core layer shows better immunity against self-heating effect because of its superior thermal conductivity [11]. When positive back-bias of 15 V is applied to the bottom silicon substrate, the potential is effectively transferred from the bottom to the top layer owing to the high electrical conductivity of the metallic layer. As back-biasing of V-NAND is possible, there is no need to apply complicated erasing configurations such as those in the GIDL method.

Fig. 5 shows the extracted potential along the BL. The potentials of both the conventional and the proposed structure were identically extracted at the surface of the metallic core layer. In the case of the conventional 3D V-NAND, voltage drop along the BL was 1.4 V per WL due to the high resistance of SiO_2. Hence, actually, back-biasing is impossible under the conventional structure. However, it was observed that the voltage drop was negligibly small under the proposed NAND structure owing to the low resistance of the inserted metallic layer. In the case of the proposed structure, extracted voltage drop at the 10th floor was only 20 mV. Based on these results, it can be inferred that erasing of electrons by aid of back-biasing can be further boosted if the back-biasing potential is higher than 15 V.

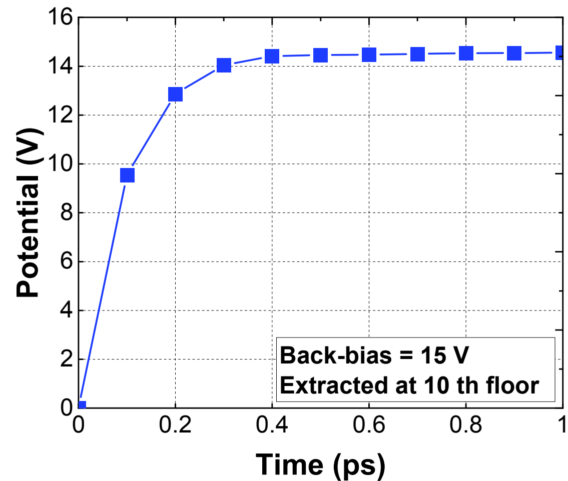

Fig. 6. Time-dependent characteristic of proposed V-NAND string at surface of metallic core layer.

However, time-dependent voltage characteristics should be confirmed to estimate the minimum time required for back-biasing, as shown in Fig. 6. The potential reached steady-state within 0.5 ps and was negligibly short compared with the erasing speed as CTL is approximately hundreds of μs to ms. As a result, even when the proposed structure and erasing configuration are applied for higher stories of a NAND string (e.g., 512 floors), the time delay is not problematic.

Fig. 7 shows a simulated energy band diagram of the conventional and the proposed V-NAND strings with respect to back-biasing. Sentaurus TCAD simulator was

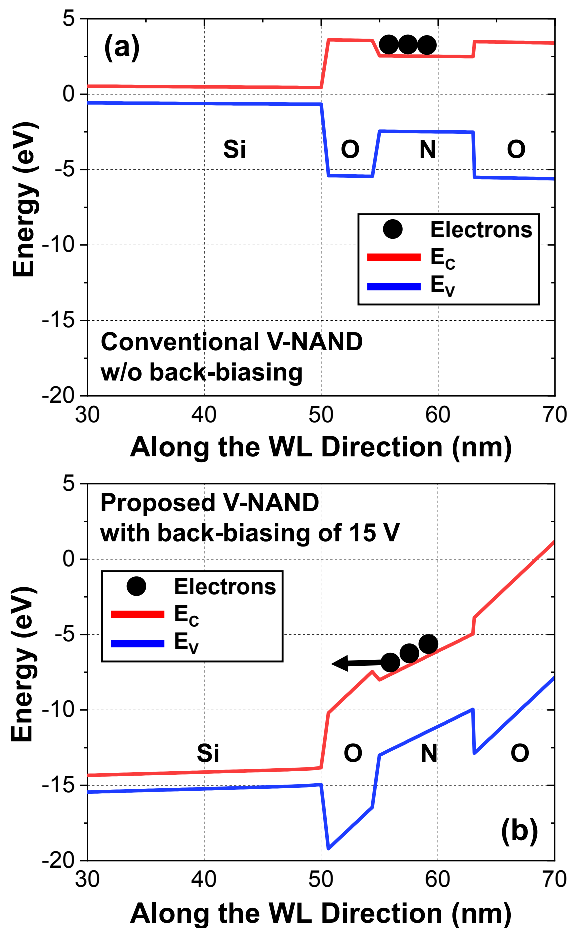

Fig. 7. Simulated energy band diagram of (a) conventional, (b) proposed V-NAND string during erasing configuration.

utilized for simulations. In the conventional V-NAND string, voltage transfer from substrate to BL is difficult. Hence, erasing configuration at high story cells (e.g., 10th floor) cannot be improved by back-biasing, as shown in Fig. 7(a). In contrast to the conventional V-NAND, the proposed structure contains a metallic core layer in the middle of macaroni filler. Hence, voltage transfer from substrate to BL is possible through the metallic layer. As a result, electrons stored at the CTL can be effectively erased through the tunneling oxide, as shown in Fig. 7(b).

IV. Conclusion

Multi-layered macaroni filler was newly proposed for improvement of erase efficiency in V-NAND. Potential distribution along the bit-line (BL) direction was investigated based on simulation studies. It was confirmed that back-biasing is possible even with the gate-all-around (GAA) device structure. The proposed V-NAND structure showed uniform back-biasing potential, regardless of stories of word-lines (WL), because of the high electrical conductivity of the metallic core layer. Stored electrons can be effectively removed from the charge trap layer (CTL) by aid of applied back-biasing. As a result, proposed multi-layered macaroni filler can improve erase efficiency in V-NAND without large modification of fabrication process or layout. However, precise gap filling during device fabrication, seems difficult even use of atomic layer deposition (ALD). Hence, there might be a trade-off between erasing performance and fabrication cost.

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