

Electrical Performances of GaN-based Vertical Trench MOSFETs with Cylindrical and Hexagonal Structure

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Abstract—In this paper, we designed and analyzed the electrical performances of gallium-nitride (GaN)-based vertical trench metal-oxide-semiconductor field-effect-transistors (MOSFETs) using three-dimensional technical computer-aided design (3-D TCAD) simulation. The cylindrical device is generally considered as superior device than the polygonal devices because it has better gate controllability. In the case of GaN-based vertical devices, however, the cylindrical device performs inferiorly to the hexagonal device in terms of crystal directions for the GaN sidewall plane such as m-plane (1-100), a-plane (11-20), and c-plane (0001). The simulation results provide an understanding and design guidelines for which electrical properties of trench FETs are affected by cross-section shape.

Index Terms—Gallium nitride (GaN), 3D architecture, field-effect transistor (FET), vertical transistor, power transistor

I. INTRODUCTION

The demand for wide bandgap semiconductors has dramatically increased in application fields such as electric vehicles, the military, and national defense.

Therefore, the development of next-generation power devices based on wide bandgap materials has become an important issue [1, 2]. Gallium-nitride (GaN) has the high critical electric field and the high electron mobility due to the two-dimensional electron gas (2-DEG) in the heterostructure of AlGaN/GaN, and it is suitable for power electronics [3, 4]. However, GaN devices with the lateral channel are not suitable for extremely high-power devices. Because the lateral GaN devices require a long gate-drain distance to achieve high threshold voltage (V_{th}) and high breakdown voltage (V_B), it results in the increase of device area. Otherwise, the vertical device has the advantage of high V_B and wide drift current region without increasing the chip size [5-8]. Therefore, vertical GaN devices could be promising candidate device for high-power electronic applications. For general vertical devices, the cylindrical device is adopted for its excellent gate controllability [9, 10]. However, for vertical GaN devices, the performance is highly dependent on the orientation of the sidewall plane. GaN has a wurtzite crystal structure and has various sidewall planes such as m-plane (1-100), a-plane (11-20), and c-plane (0001) [11]. Many studies have reported that the m-plane outperforms the a-plane [12, 13]. However, a direct comparison between a cylindrical device with mixed planes and a hexagonal device with a single crystal plane has not yet been reported for GaN-based vertical trench MOSFETs.

In this study, we present the electrical characteristics of GaN-based vertical trench MOSFETs based on cylindrical and hexagonal structures. Through the 3-D simulations, the electrical performances of GaN-based vertical trench MOSFETs are extracted and evaluated in

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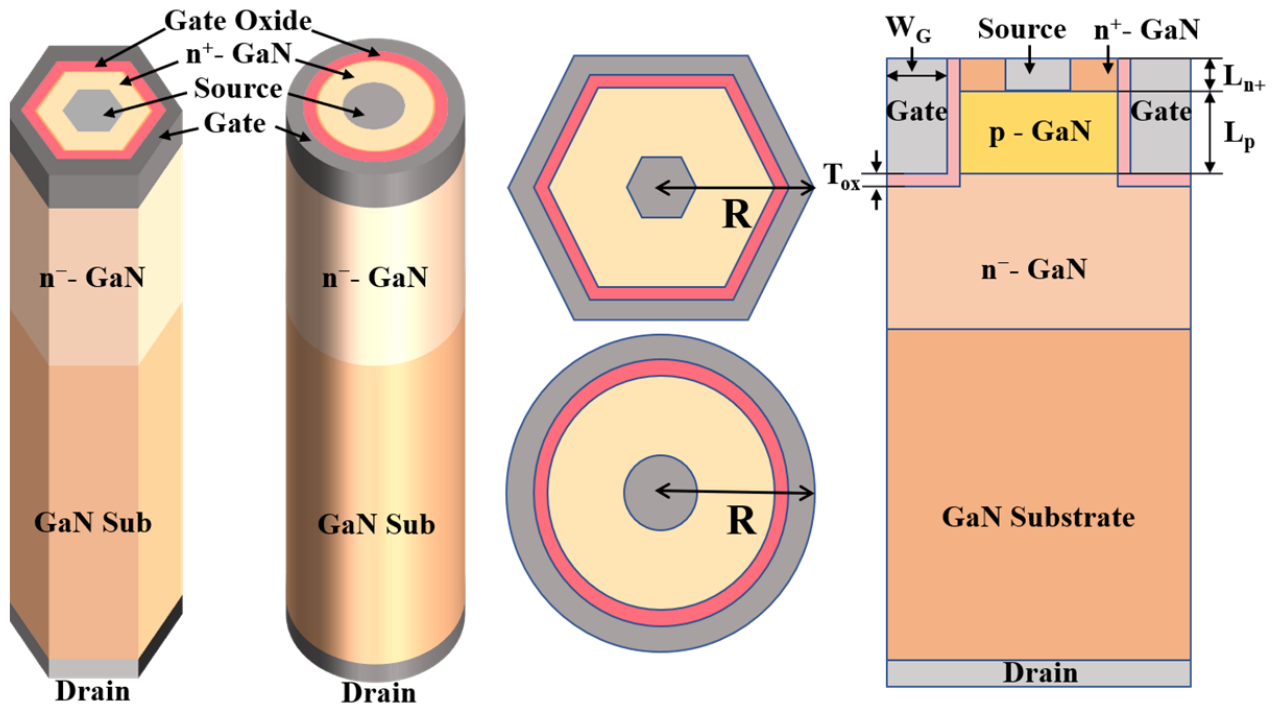


Fig. 1. 3-D and cross-sectional schematic diagrams of the hexagonal and the cylindrical structure.

Table 1. Parameters for vertical GaN trench MOSFET

Parameter	Value
Gate Width (W_G)	1 μm
Gate Oxide (Al_2O_3) Thickness (T_{ox})	80 nm
n^+ -GaN Length (L_{n^+})	200 nm
p -GaN Length (L_p)	700 nm
n^- -GaN Length	13 μm
n^+ -GaN Doping Concentration	$1 \times 10^{18} \text{ cm}^{-3}$
p -GaN Doping Concentration	$2 \times 10^{18} \text{ cm}^{-3}$
n^- -GaN Doping Concentration	$9 \times 10^{15} \text{ cm}^{-3}$
n^+ -GaN Substrate Doping Concentration	$6 \times 10^{18} \text{ cm}^{-3}$
Hexagonal Cross-sectional Area (A_H)	137.32 μm^2
Cylindrical Cross-sectional Area (A_C)	166.04 μm^2
Radius (R)	7.27 μm

terms of the current density, V_{th} , and on-resistance (R_{on}) for both cylindrical and hexagonal devices.

II. DEVICE STRUCTURE AND SIMULATION

Fig. 1 shows the schematic diagrams of the hexagonal and cylindrical cell structures of GaN-based vertical trench MOSFETs [14]. The geometric parameters are summarized in Table 1. The epitaxial structure including the GaN substrate consists of a 13 μm -thick n^- -GaN drift layer, a 700 nm-thick p-GaN channel layer, and a 200

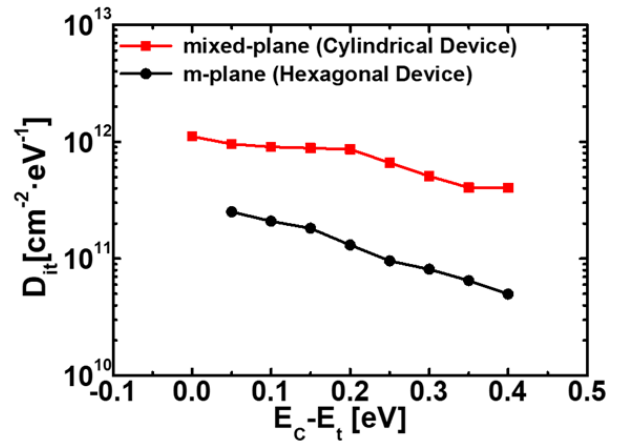


Fig. 2. Interface trap density and trap energy level of $\text{Al}_2\text{O}_3/\text{GaN}$ for m-plane and mixed-plane.

nm-thick n^+ -GaN layer. The n-type doping concentration of n^+ -GaN and n^- -GaN are $6 \times 10^{18} \text{ cm}^{-3}$ and $9 \times 10^{15} \text{ cm}^{-3}$, respectively. The p-type doping concentration of p-GaN is $2 \times 10^{18} \text{ cm}^{-3}$. 80 nm-thick Al_2O_3 is used for the gate dielectric [15]. This simulation assumes that all acceptors in the p-GaN layer are ionized. In addition, a channel is formed in the p-GaN layer to operate as a conventional enhancement mode transistor. The radius of both devices is equal to 7.27 μm to compare the electric field at the same corner.

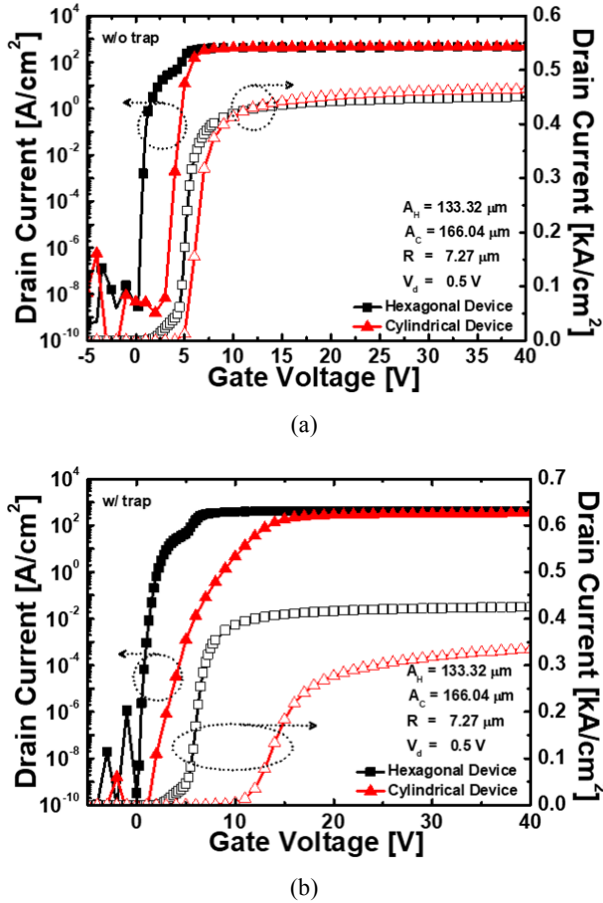


Fig. 3. Linear and logarithmic transfer I_d - V_g characteristics for the hexagonal and the cylindrical devices at $V_d = 0.5$ V: (a) without interface trap, (b) with interface trap.

The c-plane of GaN is not suitable for the normally-off operation because spontaneous polarization occurs as a polar plane. Generally, the a-plane or m-plane is used as a non-polar plane when fabricating the vertical GaN devices because they can achieve high V_{th} [16, 17]. Fig. 2 shows the Al_2O_3 /GaN interface trap densities for the m-plane and the mixed-plane [18]. The hexagonal device consists of six m-plane sidewalls, and the cylindrical device consists of sidewalls with a mixed-plane of m-plane and a-plane, rather than a single crystal plane. The mixed-plane has higher interface traps than the m-plane because the a-plane has a higher trap density than the m-plane [13]. These simulations include various physical models such as the Fermi-Dirac model, the Shockley-Read-Hall recombination model, the low field mobility model, the high field mobility model, and the shock ionization model, which were applied to increase simulation's accuracy.

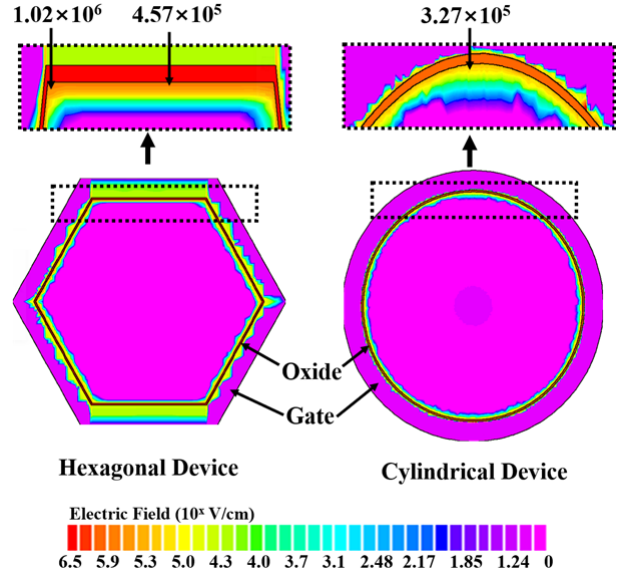


Fig. 4. Simulation profiles of the hexagonal and the cylindrical devices at $V_g = 40$ V showing electric field.

III. RESULT AND DISCUSSION

Fig. 3 shows the drain current (I_d)-gate voltage (V_g) characteristics for the hexagonal and the cylindrical GaN-based trench MOSFETs at drain voltage (V_d) = 0.5 V. The I_d is normalized by the cross-sectional area of the device. Fig. 3(a) is the I_d - V_g curve for devices without the interface trap. The V_{th} for the hexagonal and the cylindrical devices in this case are 4.37 V and 4.99 V, and the I_d are 0.450 kA/cm², and 0.464 kA/cm² at $V_g = 40$ V. The hexagonal device has the smaller perimeter and cross-sectional area than the cylindrical device, so the channel forms faster and has a lower V_{th} . In addition, the hexagonal device such as angled device, the V_{th} is lower because the electric field is focused on the corner due to the corner effect, and channel forms quickly at the corner [19]. The cylindrical device has higher I_d than the hexagonal device due to excellent gate controllability. Fig. 3(b) is the I_d - V_g curve for devices with the interface trap. The V_{th} of the hexagonal and the cylindrical devices in this case are 5.12 V and 11.15 V, and the I_d are 0.425 kA/cm² and 0.335 kA/cm² at $V_g = 40$ V. Due to the influence of the interface traps on both devices, the V_{th} is increased and the I_d is decreased. The cylindrical device is more affected by interface traps than the hexagonal device, due to the inclusion of an a-plane with high interface traps. Therefore, despite the excellent gate controllability of the cylindrical device, the electrical

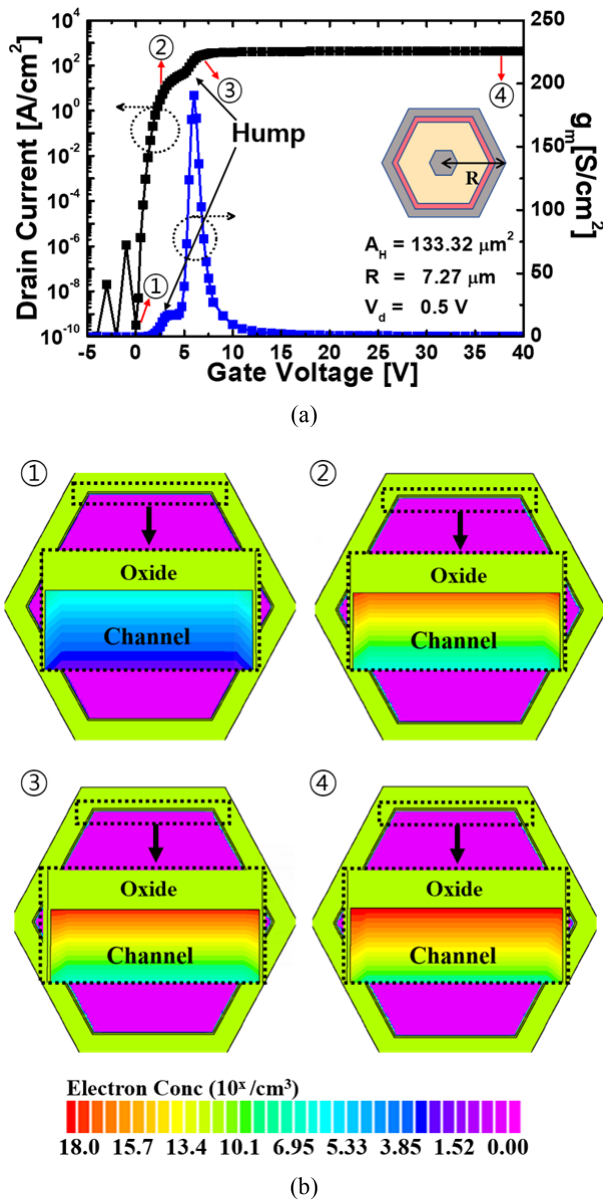


Fig. 5. (a) Logarithmic transfer I_d - V_g and transconductance g_m - V_g characteristics for the hexagonal device, (b) simulation profiles of cross-section showing electron concentration.

performance is inferior to the hexagonal device.

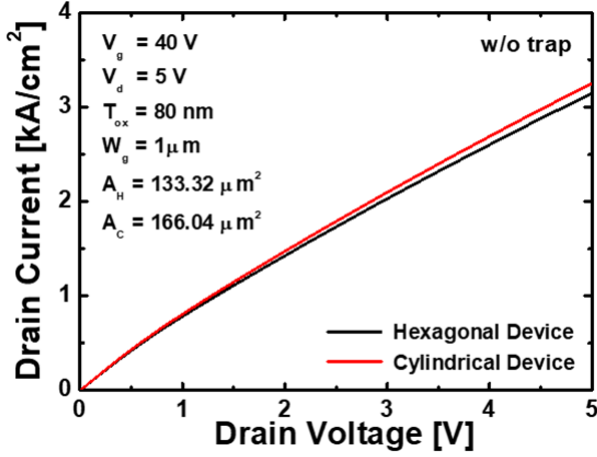
Fig. 4 shows the electric fields of the hexagonal and the cylindrical devices at $V_g = 40$ V. The cylindrical device has a smooth perimeter, which leads to a uniform electric field along the surface. On the other hand, the hexagonal device, the electric field is concentrated at the corners due to the sharp corners, as a result having a non-uniform electric field along the surface. Specifically, the electric field of the hexagonal device is 1.02 MV/cm at the corner and 0.46 MV/cm at the edge. Although the electric field of the cylindrical device is slightly different,

the result is almost uniform at 0.33 MV/cm.

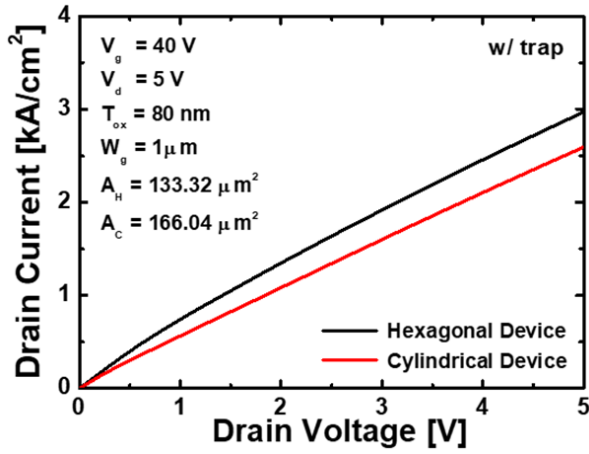
Fig. 5(a) shows the logarithmic I_d - V_g and transconductance (g_m)- V_g characteristics of the hexagonal device. Fig. 5(b) shows the cross-sectional electron concentration at each point. As shown in Fig. 5(a), the hump shape occurs in the I_d - V_g curve of the hexagonal device. The inversion layer is not formed and the current does not flow well when V_g is 0 V, as shown in Fig. 5(b). The inversion layer begins to be formed at the corner when V_g increases until just before the formation of the hump. When additional V_g is applied and the hump shape occurs, a sufficient inversion layer is formed on the edges as well as the corners, allowing more current to flow. Finally, at $V_g = 40$ V, the inversion layer of high electron concentration is formed at the edges and corners. This is due to the corner effect shown in Fig. 4, which is the reason the channel is formed rapidly at the corners of the hexagonal device, resulting in lower V_{th} and a difference in the formation of an inversion layer between edges and corners, resulting in the hump shape occurs.

Fig. 6 shows the I_d - V_d characteristic of the hexagonal and the cylindrical devices. The R_{on} is calculated in the linear region of $V_d = 0.5$ V and $V_g = 40$ V. Fig. 6(a) for devices without the interface trap shows that the cylindrical device has a higher current density than the hexagonal device. Also, the R_{on} is 1.16 $m\Omega \cdot cm^2$ of the cylindrical device, which is lower than 1.20 $m\Omega \cdot cm^2$ of the hexagonal device. However, Fig. 6(b) for devices with the interface trap shows that the hexagonal device has a higher current density than the cylindrical device. This means that the hexagonal device has higher channel mobility and lower R_{on} than the cylindrical device. The calculated R_{on} is 1.24 $m\Omega \cdot cm^2$ of the hexagonal device and 1.66 $m\Omega \cdot cm^2$ of the cylindrical device. This is because the a-plane included in the mixed-plane of the cylindrical device has higher trap density and lower interface quality than the m-plane. These results indicate that the GaN-based vertical trench MOSFET is highly dependent on the orientation of the channel sidewall plane.

Fig. 7 shows the off-state I_d - V_d characteristics of the hexagonal and the cylindrical devices when V_g is 0 V. The V_B of the hexagonal and the cylindrical devices are 2,660 V and 2,682 V, respectively. The V_B of the hexagonal device is slightly lower than that of the



(a)



(b)

Fig. 6. Output I_d - V_d characteristics for the hexagonal and the cylindrical devices at $V_g = 40$ V: (a) without interface trap, (b) with interface trap.

cylindrical device because the electric field is focused on the corners. The hexagonal device has not only better electrical performances than the cylindrical device but also the V_B of only about 1% lower than the cylindrical device.

The V_{th} , I_d , and R_{on} of the analyzed hexagonal and cylindrical devices are summarized in Table 2. As shown in Table 2, the cylindrical device shows superior electric performances when there are no interface traps. However, considering the interface traps along the crystal plane orientation, the electrical performances of both devices are degraded. Specifically, the cylindrical device shows inferior electrical performances as compared to the hexagonal device due to many interface traps.

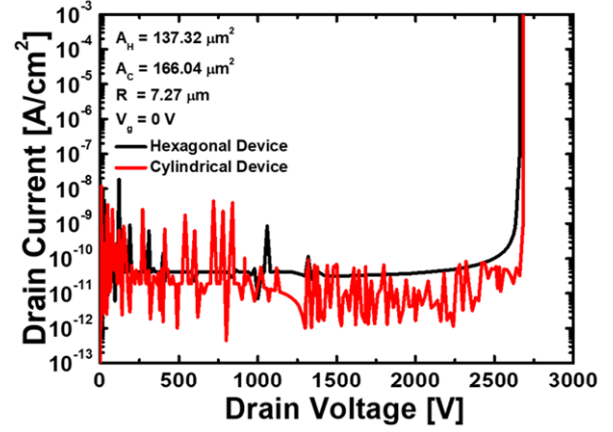


Fig. 7. Off-state I_d - V_d Characteristic for the hexagonal and the cylindrical devices at $V_g = 0$ V.

Table 2. Parameters Metrics of the analyzed devices

Electrical Performance Metrics	Hexagonal device		Cylindrical device	
	w/o trap	w/ trap	w/o trap	w/ trap
V_{th} [V]	4.37	5.12	4.99	11.15
I_d [kA/cm ²]	0.450	0.425	0.464	0.335
R_{on} [m Ω ·cm ²]	1.20	1.24	1.16	1.66

IV. CONCLUSIONS

This study analyzed the effect of crystal orientations for the sidewall plane on the electrical performances of GaN-based vertical trench MOSFETs with hexagonal and cylindrical structures. The GaN-based vertical trench MOSFET's electrical performances are highly dependent on the orientation of the sidewall plane of the channel. Electrical performances decreased in both devices due to the influence of the interface traps. However, it is shown that the hexagonal device consists of m-plane and has fewer interface traps than the cylindrical device consists of mixed-plane, it has better electrical performances despite the negative effects due to the corner effect. Therefore, to enhance the performances of the device, it is advantageous to design the crystal orientation toward the m-plane. The results of this study provide insight into the electrical properties of GaN-based vertical trench MOSFETs, as well as design guidelines.

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REFERENCES

- [1] Jang, Won-Ho, et al. "P-GaN Gated AlGaIn/GaN E-mode HFET Fabricated with Selective GaN Etching Process." *JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE*. pp. 485-490. Dec 2020
- [2] Oduangvilai, Konepachith, et al. "Study of Gate Leakage Current on AlGaIn/GaN MOSHEMTs with Atomic Layer Deposited Al₂O₃ Gate Oxide." *JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE*. pp. 540-550. Dec 2019
- [3] Choton, Jahid Chowdhury, et al. "Design and Characterization of 2DEG Structure of a Gallium Nitride HEMT." *IEEE 2019 International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST)*. pp. 486-489. Feb 2019.
- [4] Syaranamual, Govindo J., et al. "Role of two-dimensional electron gas (2DEG) in AlGaIn/GaN high electron mobility transistor (HEMT) ON-state degradation." *Microelectronics Reliability* vol. 64 no. 21 pp. 589-593 Sep 2016
- [5] Kanechika, Masakazu, et al. "A vertical insulated gate AlGaIn/GaN heterojunction field-effect transistor." *Japanese Journal of Applied Physics* Vol. 46 pp. L503-L505 May 2007
- [6] Chowdhury, Srabanti, Brian L., et al. "Enhancement and depletion mode AlGaIn/GaN CAVET with Mg-ion-implanted GaN as current blocking layer." *IEEE Electron Device Letters* Vol. 29 no. 6 pp. 543-545 Jun 2008
- [7] Sun, Min, et al. "High-performance GaN vertical fin power transistors on bulk GaN substrates." *IEEE Electron Device Letters* Vol. 38 no. 4 pp. 509-512 Apr 2017.
- [8] Oka, Tohru, et al. "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV." *Applied Physics Express* Vol. 7 no. 2 p. 021002 Jan 2014
- [9] Takato, H., et al. "High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs." *IEEE Technical Digest., International Electron Devices Meeting*. pp. 11-14 Dec 1988
- [10] Kim, Sung Yoon, et al. "Electrical characteristics of enhancement-mode n-channel vertical GaN MOSFETs and the effects of sidewall slope." *Journal of Electrical Engineering and Technology* Vol. 10 no. 3 pp. 1131-1137 May 2015 Aug 2016
- [11] Wang, T. "Topical Review: Development of overgrown semi-polar GaN for high efficiency green/yellow emission." *Semiconductor Science and Technology* Vol. 31 no. 9 p. 093003
- [12] Gupta, Chirag, et al. "Comparing electrical performance of GaN trench-gate MOSFETs with a-plane and m-plane sidewall channels." *Applied Physics Express* Vol. 9 no. 12 p. 121001 Nov 2016
- [13] Jia, Ye, et al. "Interface characterization of atomic layer deposited high-k on non-polar GaN." *Journal of Applied Physics* Vol. 122 no. 15 p. 154104 Jun 2017
- [14] Oka, Tohru, et al. "1.8 mΩ·cm² vertical GaN-based trench metal-oxide-semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation." *Applied Physics Express* Vol. 8 no. 5 p. 054101 Apr 2015
- [15] Chang, Y. C., et al. "Inversion-channel GaN metal-oxide-semiconductor field-effect transistor with atomic-layer-deposited Al₂O₃ as gate dielectric." *Applied Physics Letters* Vol. 93 no. 5 p. 053504 Jun 2008
- [16] Fu, Houqiang, et al. "Nonpolar vertical GaN-on-GaN p-n diodes grown on free-standing m-plane GaN substrates." *Applied Physics Express* Vol. 11

no. 11 p. 111003 Oct 2018

- [17] Fujiwara, Tetsuya, et al. "Enhancement-mode m-plane AlGaIn/GaN heterojunction field-effect transistors." *Applied Physics Express* Vol. 2 no. 1 p. 011001 Jan 2009
- [18] Thingujam, Terirama, et al. "A simulation study on the effects of interface charges and geometry on vertical GAA GaN nanowire MOSFET for low-power application." *IEEE Access*. Vol. 9 pp. 101447-101453 Jul 2021
- [19] De Michielis, Luca, et al. "Corner effect and local volume inversion in SiNW FETs." *IEEE transactions on nanotechnology* Vol. 10 no. 4 pp. 810-816 Sep 2010



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