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Prediction Methodology for Next-generation Device Characteristics using Machine Learning

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Abstract—**In this article, we propose a prediction methodology for next-generation device characteristics for process design kit (PDK) models that utilize various machine learning algorithms to achieve high accuracy and reduction of development turn-around time (TAT). The Berkeley short-channel IGFET model (BSIM) is used for generating datasets, while *n*-channel MOSFET compact model is used for peripheral circuits in dynamic random-access memory (DRAM) technology. Datasets for training comprise device characteristics that use compact models in present-generation products. In addition, a compact model of next-generation products is used for validating datasets. We demonstrate that our prediction methodology using random forest regression provides high accuracy of less than 0.7% RMSE and reduces development TAT.**

Index Terms—**Device characteristics, machine learning, compact model**

I. INTRODUCTION

Over the past decades, the continued scaling down of metal-oxide-semiconductor field-effect-transistors (MOSFETs) has been driving dynamic random-access memory (DRAM) technology with high performance and low power consumption [1]. However, with the scaling down of transistors reaching physical limitations, the prediction of electrical characteristics in transistors has become challenging owing to diverse unpredictable effects of new process technologies [2]. Especially, predicting the electrical characteristics of transistors used in DRAM technology peripheral regions is very important because of the design of operations in peripheral circuits [3]. Hence, the prediction of device characteristics used in compact models for process design kit (PDK) development, which connects the process technology and circuit design, is becoming increasingly important in reducing the product development period. This compact model development is limited by various secondary effects induced by new process technologies as well as the increase in number of model parameters. In particular, the increase in number of model parameters contribute to the complexity of PDK models, resulting in a long development time and reduced accuracy. Thus, the prediction accuracy of PDK model device characteristics gradually decreased following an increase in model complexity and development time [4]. Therefore, to improve the prediction accuracy for next generation device characteristics using peripheral circuit in DRAM technology, we propose a prediction methodology based on compact models using a machine learning algorithm.

II. DATA GENERATION AND MACHINE LEARNING ALGORITHM

In this study, we utilized BSIM version 4.8 to generate datasets for training and validating the machine learning models. The BSIM model consists of physics-based numerical equations for gate channel length and width in MOSFET, including secondary effects such as short

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Table 1. Measured conditions of seven ET items of *n*-channel MOSFET compact models used in HSPICE simulation

Extracted seven ETs	Feature
V_{th}	Extracted by g_m method
Idsat	$V_{DS}=V_{GS}=V_{DD}$
Idsat2	$V_{DS}=V_{DD}$, $V_{GS}=V_{DD}/2$
Idmid	$V_{DS}=V_{DD}/3$, $V_{GS}=V_{DD}$
Idmid2	$V_{DS}=V_{DD}/2$, $V_{GS}=V_{DD}/2$
Idlin	$V_{DS}=0.05$V, $V_{GS}=V_{DD}$
Ioff	$V_{DS}=V_{DD}$, $V_{GS}=0.0$ V

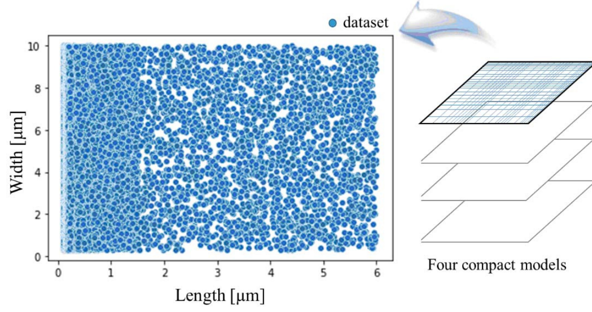

Fig. 1. Total dataset generated by compact models within guaranteed L and W.

channel effect, narrow width effect, drain induced barrier lowering, and gate induced drain leakage. Based on BSIM compact models for three present-generation products and one next-generation product, we extracted seven electrical test (ET) items using device electrical characteristics in *n*-channel MOSFET, namely threshold voltage (V_{th}), saturation drain current (Idsat and Idsat2), mid-region drain current (Idmid and Idmid2), linear region drain current (Idlin), and off-current (Ioff), as listed in Table 1. Seven ETs were extracted from the guaranteed channel length (L) and width (W) for 1,000 points using Synopsys HSPICE (P-2019.06) [5], as shown in Fig. 1. Total 28,000 electrical characteristics were extracted using each compact model for training and validating data. The seven ETs extracted from present-generation and next-generation products were used as training and validating data, respectively. As the device characteristics of present-generation products were used by a 17 nm process compact model, 15 nm process compact models for next-generation device characteristics were validated. Mature compact models for predicting device characteristics were used in 17 nm and 15 nm process products, respectively. In our prediction algorithm, L, W, and design rule are the input features, and the seven ETs are the outputs, as shown in

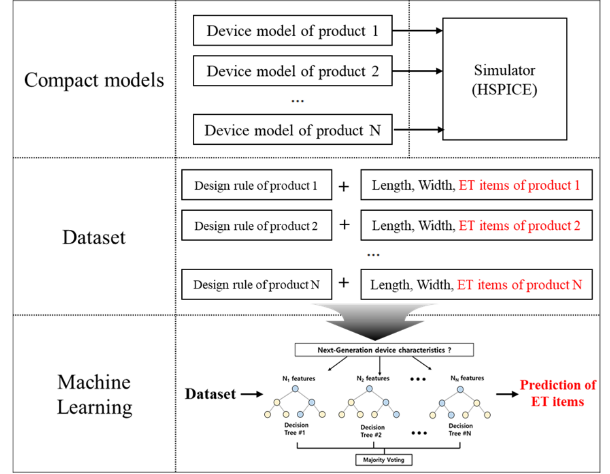

Fig. 2. Machine learning framework used in this study.

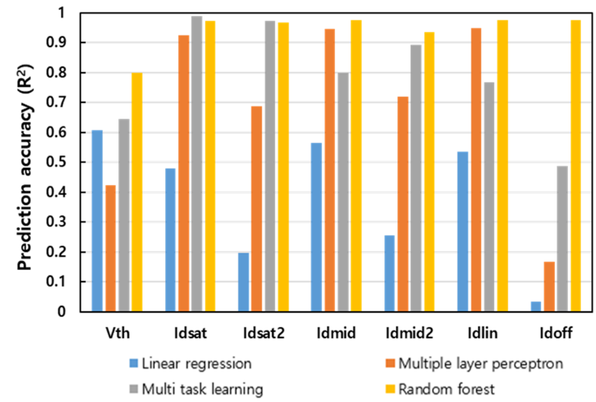

Fig. 3. Comparison of the prediction accuracy (R^2) of various learning methods for predicting next-generation device characteristics.

Fig. 2. The seven ETs extracted from present-generation products were trained by corresponding *n*-channel MOSFET in 17 nm process products using peripheral circuits. Then, the input features of 15 nm process products, such as design rule, L, and W for validation were provided, from which our predicting algorithm predicted seven ETs of 15 nm process products. In addition, the SPICE simulator running time for each model was within a minute and could be carried out in less than thirty minutes to generate a total dataset.

III. Result and Discussion

Fig. 3 shows a comparison of the prediction accuracy with diverse learning methods in terms of the coefficient of determination values (R^2) of seven ETs. We evaluated four learning algorithms including linear regression,

multiple layer perceptron, multitask learning, and random forest regression. The results showed that random forest regression had the highest R^2 in all ETs. It predicted V_{th}, Idsat, Idsat2, Idmid, Idmid2, Idlin, and Idoff with an R^2 of 0.800, 0.971, 0.968, 0.976, 0.934, 0.975, and 0.976, respectively. In addition, all predicted ETs exhibited high accuracies within 0.7% normalized root mean square error (RMSE). In this study, RMSE was calculated using normalized data, as shown in Eq. (1) below:

$$Normalized\ x = \frac{x.value - x(\min)}{x(\max) - x(\min)} \quad (1)$$

Our predicting algorithm uses random forest regression, which is a supervised learning algorithm, employs ensemble learning methods for regression to predict next-generation device characteristics [6]. Ensemble learning method creates and classifies multiple classifier models with decision trees, and then one with the higher probability of correct answer is selected by a majority vote [6]. During the training time, several decision trees are produced. Afterwards, the majority voting is executed by prediction of all the trees by means of the outputting.

Random forest regression is suitable in predicting device characteristics because it is fast, robust and parallel [7]. Among the seven ETs, the V_{th} is difficult to estimate the length and width trends due to several effects, such as the short channel, narrow width, and reverse short channel effects. Generally, drain currents such as Idsat, Idmid, and Idlin do not vary considerably depending on the product, although the V_{th} varies greatly depending on the product. This is due to the variation in process parameters and secondary effects. Nevertheless, our prediction methodology can achieve high prediction accuracies and low error rates using random forest regression because of their robustness compared to other learning methods such as a single decision tree in finite training data, as shown in Fig. 3.

Fig. 4 shows the 3D mesh comparison of a validation set and prediction model of the channel length and width variation. The seven ETs are well matched to validation sets, as shown in Fig. 4(a) and (b). In our prediction methodology, each design rule for products enables each product to predict next-generation device characteristics.

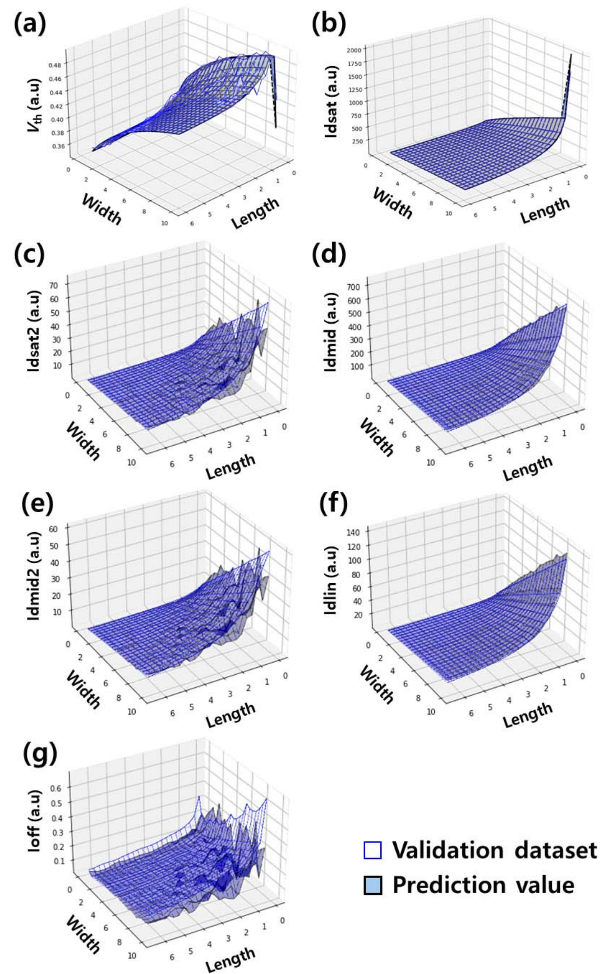

Fig. 4. 3D mesh comparison of validation set and prediction model for seven ET items (a) Vth, (b) Idsat, (c) Idsat2, (d) Idmid, (e) Idmid2, (f) Idlin, (g) Ioff.

As transistors that use peripheral circuits of DRAM products have few structural changes from generation to generation and product line to production, our proposed methodology can be applied efficiently in predicting next-generation device characteristics for circuit designs.

In this prediction methodology, simulation results show that random forest regression can capture several small and importance features, such as the relationship between the device characteristics and design parameters. Consequently, we are certain that device physics is vividly captured using our prediction methodology with a high prediction accuracy of R^2. Furthermore, our prediction time for generating electrical design rule targets including seven ETs is ~1000 times faster than conventional methods generated using human resources [4]. In this study, our prediction methodology used device structures of peripheral circuits in DRAM

technology, which had fewer structural changes from generation to generation. However, if we have a sufficient database, our prediction methodology can also be applied to logic or NAND flash memory devices.

In this study, next-generation device characteristics including seven ETs were well predicted using various device compact models with our prediction methodology. The predicted device characteristics were used to establish next-generation device compact models. Therefore, predicting device characteristics in our prediction methodology with a high accuracy and reduced development TAT is one of the important areas in design technology co-optimization for DRAM technologies.

IV. CONCLUSION

In this paper, we presented the possibility of predicting next-generation device characteristics by using machine learning with PDK models. Random forest regression algorithm was used to predict seven ET items using high prediction accuracy of R^2, within 0.7% RMSE. Therefore, our predicting methodology provides a new perspective on predicting next-generation device characteristics with high accuracy and reduced development TAT.

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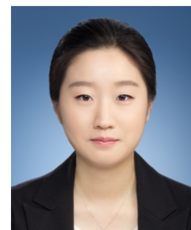

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