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Fabrication and Performances of Recessed Gate AlGaN/GaN MOSFETs with Si_3N_4/TiO_2 Stacked Dual Gate Dielectric

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***Abstract*—In this paper, a recessed gate AlGaN/GaN metal-oxide-semiconductor field-effect-transistor (M-OSFET) with Si_3N_4/TiO_2 stacked dual gate dielectric was proposed and fabricated to improve the current drivability. Normally-off operation with a V_{th} of 1.81 V was obtained using a Cl_2-based gate recess etching process. Dual gate dielectric technology was used to improve the current characteristics that can be degraded by damage resulting from gate recess etching. Compared to the single gate dielectric (Si_3N_4 = 30 nm)-based device, the $I_{D,max}$ and g_m of the dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based device were improved by 292% and 195%, respectively. Moreover, the R_{on} and SS were improved by 62% and 68%, respectively. Breakdown voltage decreased by 1.4%, but there was minor difference. Therefore, the technique of depositing Si_3N_4 on GaN and then stacking high-k TiO_2 can improve the current characteristics by increasing the capacitance through a simple process. As such, the recessed gate AlGaN/GaN MOSFETs with Si_3N_4/TiO_2 stacked dual gate dielectric has the potential for high-efficiency power devices.**

***Index Terms*—GaN, AlGaN, dual gate dielectric, silicon nitride (Si_3N_4), titanium dioxide (TiO_2), normally-off, recessed gate technique**

I. INTRODUCTION

With the recent advances in technology, the development of applications requiring high power and efficiency, such as computers, electric vehicles, solar power, and smart grids is emerging. Electric vehicles require high-performance power semiconductor devices. Gallium nitride (GaN) has attracted great attention for applications in power electronics due to its wide bandgap, high critical electric field, and thermal resistance [1-5].

GaN-based high electron mobility transistors (HEMT) have high breakdown voltage due to the material properties of GaN. In addition, since the on-resistance is reduced via the two-dimensional electron gas (2DEG) with high electron mobility caused by the AlGaN/GaN junction as a channel, it is suitable for high-frequency and high-power semiconductors. However, in the general AlGaN/GaN HEMT, the 2DEG layer is used as a channel to have a negative threshold voltage (V_{th}), so power consumption is high. Therefore, it is very important for the design to have a positive V_{th} to reduce the power loss [6].

Recently, many technologies for realizing normally-off HEMT through various methods such as gate injection transistor (GIT) [7-9], fluorine plasma treatment [10-12], and recessed gate metal insulator semiconductor (MIS) structure [13-17] have been studied. GIT is difficult to

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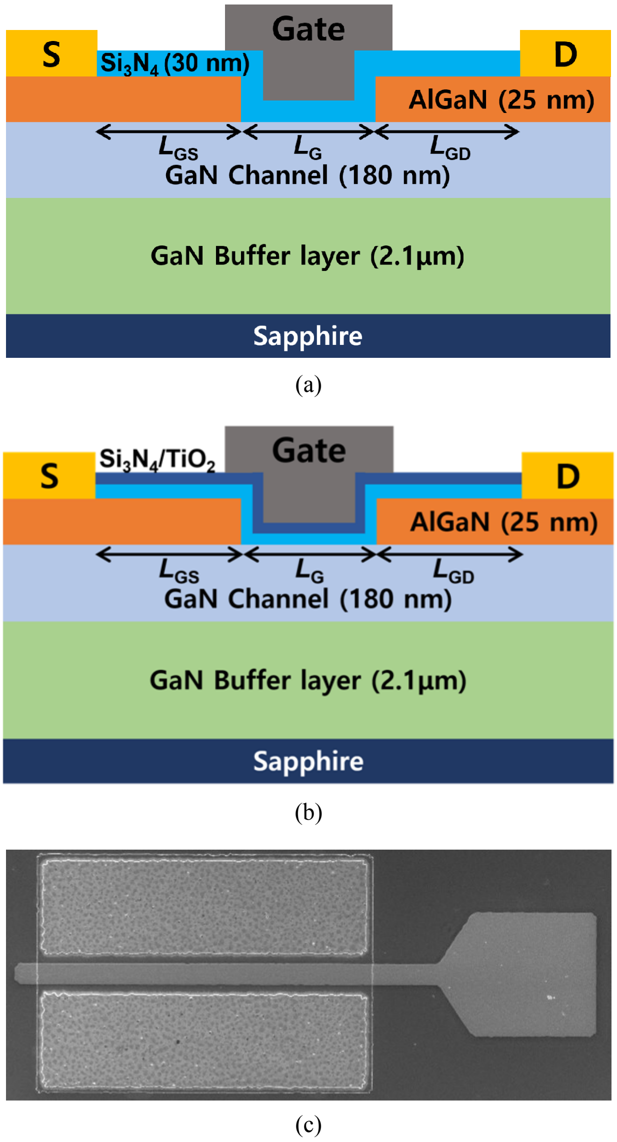


Fig. 1. The schematic cross-sections of the recessed gate AlGaN/GaN MOSFET with (a) the single gate dielectric, (b) dual gate dielectric, (c) The optical microscope image of the fabricated the recessed gate AlGaN/GaN MOSFET.

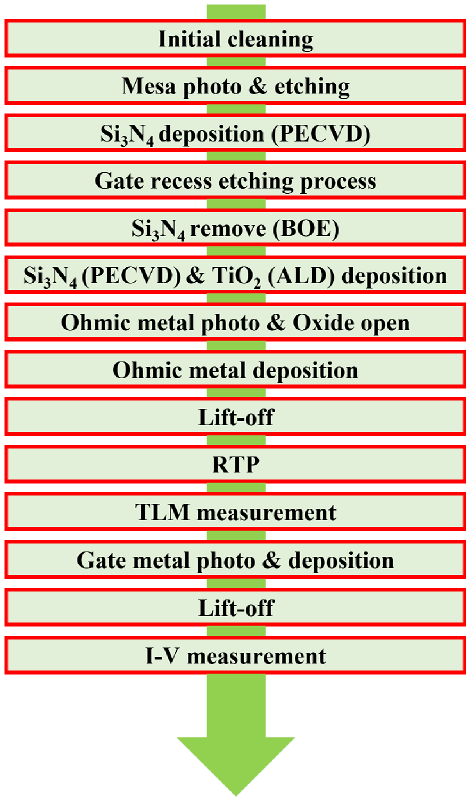


Fig. 2. Process flow of the recessed gate AlGaN/GaN MOSFET with Si_3N_4/TiO_2 stacked dual dielectric.

grow p-GaN and the output current is relatively low as compared to other structures. Additionally, when GaN is grown by metal organic chemical vapor deposition (MOCVD), it becomes n-GaN, so that it is difficult to dope the p-type to grow p-GaN. Fluorine plasma treatment is unstable at high temperatures. Conversely, the recessed gate MIS structure has a relatively simple process and high output current compared to the GIT structure. In addition, since there is an insulator under the gate, it is possible to effectively reduce the gate leakage current [18-23].

In this paper, a dual gate insulator is adopted to prevent the increase in the gate leakage current and the off-current and to improve the on-current for general recessed gate AlGaN/GaN MOSFETs. Therefore, Si_3N_4 (ε = 8.9) with relatively better interfacial properties than TiO_2 (ε = 80) was first deposited on GaN, and high-k TiO_2 was deposited on Si_3N_4 to fabricate a device. We fabricated two types of dual gate dielectric-based devices with different thicknesses of Si_3N_4 and TiO_2 (Si_3N_4/TiO_2 = 10/20 nm and 20/10 nm) and Si_3N_4 single dielectric-base device with the same process. We compared the electric characteristics of the three devices.

II. STRUCTURE AND FABRICATION

Fig. 1(a) and (b) show the schematic cross-sectional view of the single gate dielectric- and dual gate dielectric-based devices, respectively. Fig. 1(c) shows the optical microscope image of the fabricated recessed gate AlGaN/GaN MOSFET. The dual gate dielectric-based device consists of Si_3N_4 gate dielectric at the bottom and TiO_2 gate dielectric at the top. Si_3N_4 instead of TiO_2 is chosen as the material to be deposited directly on GaN as the gate leakage current increases when high-k TiO_2 is directly bonded to GaN. Later, when TiO_2 is stacked and used as a dual gate dielectric, the increased oxide capacitance can lead to a high on-state current without significant change in the gate leakage current due to the Si_3N_4/GaN junction.

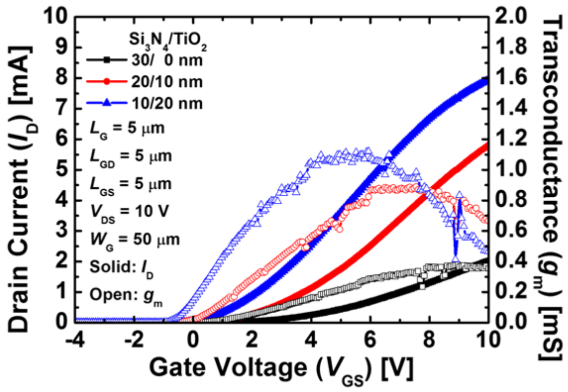
Fig. 2 shows the process flow of the recessed gate AlGaN/GaN MOSFET with Si_3N_4/TiO_2 stacked dual dielectric. The fabricated device was an epitaxial growth of GaN and AlGaN layers using MOCVD on a sapphire substrate. The thicknesses of sapphire substrate, GaN buffer, GaN channel, and AlGaN layers are 430 µm, 2.1 µm, 180 nm, and 25 nm, respectively. The Al composition in the AlGaN layer was 21%. The sheet carrier density and the electron mobility obtained by hall measurements were 8×10^{12} cm^{-2} and 1200 cm/V·s, respectively. To physically insulate each device, 380 nm depth mesa insulation was performed by Cl_2-based inductively coupled plasma-reactive ion etcher (ICP-RIE). After the mesa process, a 50 nm-thick Si_3N_4 layer was deposited via plasma enhanced chemical vapor deposition (PECVD) to be used as a hard mask in the recessed gate process. In the gate recess etching process, a 25 nm-thick AlGaN layer was etched by Cl_2-based ICP-RIE. Then, the Si_3N_4 layer used as the gate dielectric was deposited via PECVD. Subsequently, TiO_2 layer used as the gate dielectric was deposited by atomic layer deposition. Before depositing the ohmic contact metal, BOE solution was used to open the oxide at the location to enter the source and drain metals. Next, the material to be used as the ohmic contact metal of the source and drain consisting of Ti/Al/Ni/Au (25/160/40/100 nm), was deposited using an electron-beam (E-beam) evaporator. To form an ohmic contact, annealing was performed at 800°C for 30 s in the nitrogen (N_2) atmosphere. Finally, a gate metal composed of Ni/Au (40/100 nm) material was deposited using an E-beam evaporator.

III. Results and Discussion

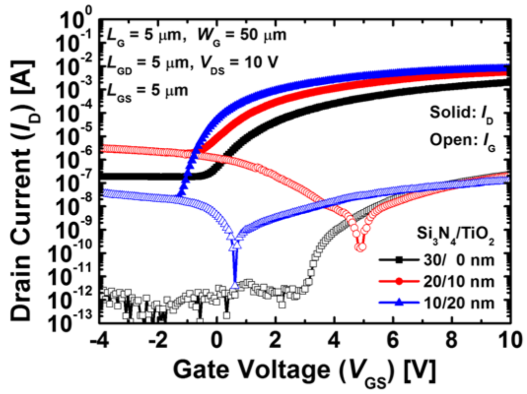
Fig. 3(a) and (b) show the transfer curve of the single gate dielectric and dual gate dielectric-based devices. The on- state drain current ($I_{D,max}$) is defined at V_{GS} = 10 V and V_{DS} = 10 V. V_{th} is obtained by linear extrapolation. A dual dielectric-based device has higher on-current and transconductance (g_m) than a single dielectric-based device. Among the two types, the dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based device exhibited the highest current characteristics, with the V_{th} of 1.81 V, $I_{D,max}$ of 7.95 mA, g_m of 1.12 mS, and subthreshold swing (SS) of 229 mV/dec. The measured electrical characteristics of the fabricated devices are summarized in Table 1. The current characteristics were improved for the dual gate dielectric because of higher capacitance than the single Si_3N_4 gate dielectric. The formula for calculating the capacitance is as follows:

Table 1. The measured electrical characteristics of the fabricated devices

Si_3N_4/TiO_2	30/0 nm	20/10 nm	10/20 nm
V_{th} [V]	4.19	3.00	1.81
$I_{D,max}$ [mA]	2.03	5.80	7.95
g_m [mS]	0.38	0.89	1.12
SS [mV/dec]	717	890	229
R_{on} [Ω·mm]	115.60	57.96	43.81
C_{ox} [nF/cm^2]	344	390	506
BV [V]	572	556	564



(a)



(b)

Fig. 3. The transfer curve of single gate dielectric and dual gate dielectric-based device with (a) g_m, (b) gate current.

$$C_{TiO_2} = \frac{\varepsilon_{TiO_2} \cdot \varepsilon_0}{t_{TiO_2}} \quad (1)$$

$$C_{Si_3N_4} = \frac{\varepsilon_{Si_3N_4} \cdot \varepsilon_0}{t_{Si_3N_4}} \quad (2)$$

$$\frac{1}{C_{total}} = \frac{1}{C_{Si_3N_4}} + \frac{1}{C_{TiO_2}} \quad (3)$$

where ε_{TiO_2} (=80) and $\varepsilon_{Si_3N_4}$ (=8) are the relative dielectric constants of TiO_2 and Si_3N_4, respectively. ε_0 is the vacuum permittivity. t_{TiO_2} and $t_{Si_3N_4}$ are the thicknesses of TiO_2 and Si_3N_4, respectively. C_{TiO_2} and $C_{Si_3N_4}$ are the capacitances of TiO_2 and Si_3N_4, respectively, and C_{total} is the total accumulation capacitance. The calculated capacitances of the single gate dielectric (Si_3N_4 = 30 nm), dual gate dielectric (Si_3N_4/TiO_2 = 20/10 nm) and dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm) were 236 nF/cm^2, 337 nF/cm^2, and 590 nF/cm^2 respectively. In MOSFET, I_D is proportional to C_{ox}, so using a dual gate dielectric increases the on-current. Therefore, compared to the single gate dielectric-based device, the $I_{D,max}$ and g_m of the dual gate dielectric-based device were improved by 292% and 195%, respectively.

Fig. 4(a) shows the $C-V$ curves of the single gate dielectric- and dual gate dielectric-based devices which with almost similar capacitance to the calculated one, and the dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based device exhibited the highest capacitance. In Fig. 4(a), the slope of the dual gate dielectric (Si_3N_4/TiO_2 = 20/10 nm)-based device was the largest, with high *SS* due to a high slope. The slope of the C-V curve is affected by the interface trap between the gate oxide and the semiconductor junction. Therefore, dual gate dielectric (Si_3N_4/TiO_2 = 20/10 nm)-based device has the highest interface trap density (D_{it}).

Fig. 4(b) shows the G_p/ω vs V_{GS} characteristics of the single gate dielectric and dual gate dielectric-based devices. D_{it} was extracted using the conductance method. The formula to calculate G_p/ω is as follows [24, 25]:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 \left(C_{ox} - C_m\right)^2} \quad (4)$$

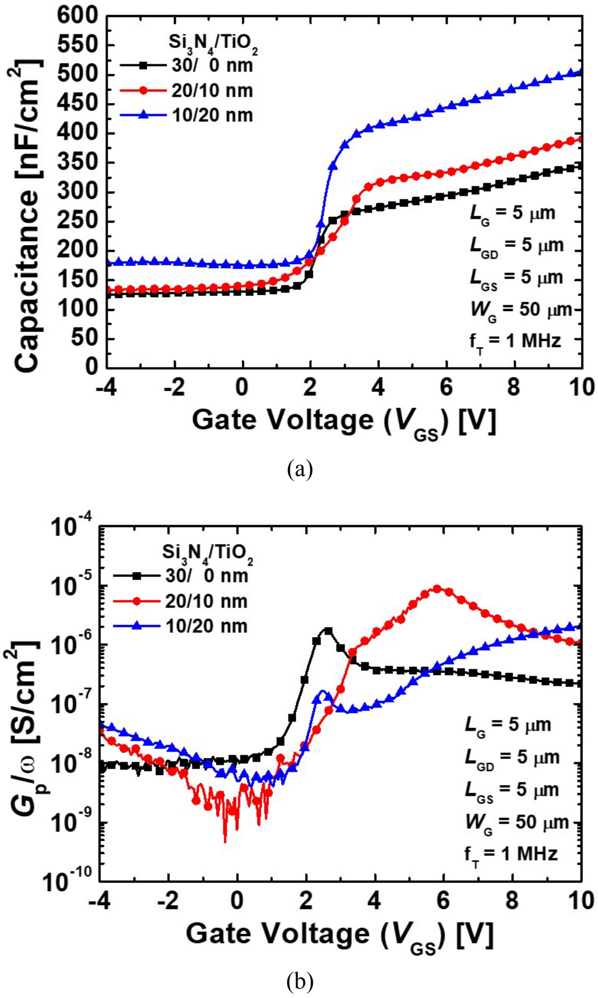
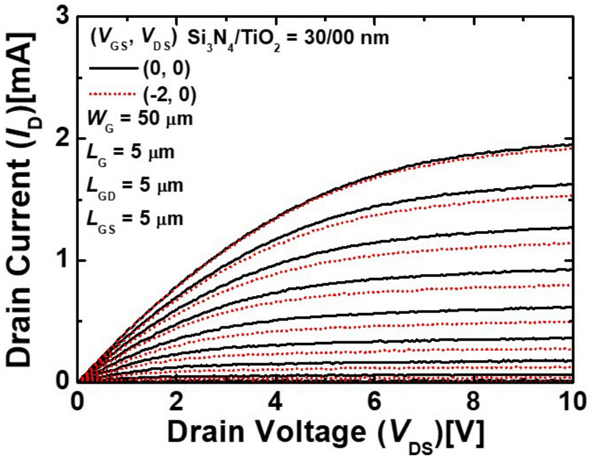


Fig. 4. (a) The $C-V$ curves, (b) G_p/ω vs V_{gs} characteristics of the single gate dielectric and dual gate dielectric-based devices.

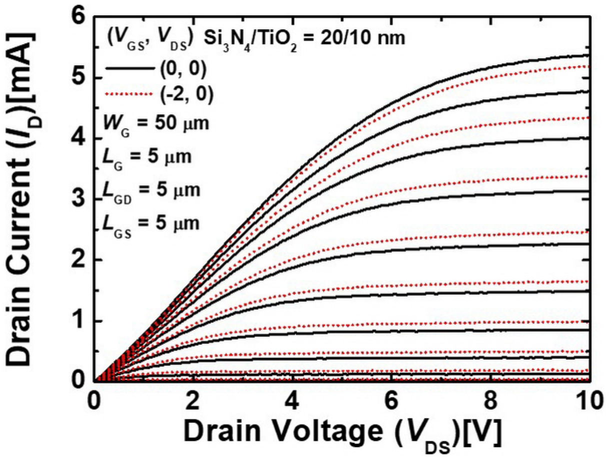
where ω (=2πf) is the angular frequency, C_{ox} is the gate oxide capacitance, G_p is the parallel conductance, G_m is the measured conductance, and C_m is the measured capacitance. Moreover, the formula to calculate D_{it} is as follows [24, 25]:

$$D_{it} = \frac{1}{0.4Aq}\left(\frac{G_p}{\omega}\right)_{max} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max} \quad (5)$$

where A is the area of the proposed device and q is the electronic charge in coulombs. D_{it} of the single gate dielectric (Si_3N_4 = 30 nm), dual gate dielectric (Si_3N_4/TiO_2 = 20/10 nm), and dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based device extracted from the Eq. (5) were 2.79 × 10^{13} cm^{-2}·eV^{-1}, 1.37 × 10^{14} cm^{-2}·eV^{-1}, and 2.53 × 10^{12} cm^{-2}·eV^{-1}, respectively.



(a)



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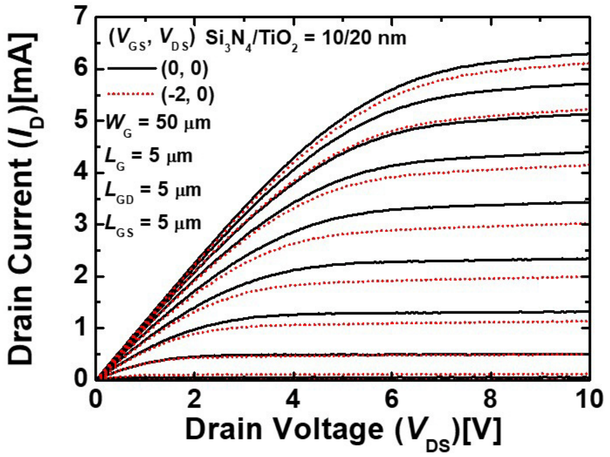


(c)

Fig. 5. The pulsed I_D−V_{DS} transfer curve of recessed gate AlGaN/GaN MOSFETs with (a) Si_3N_4 = 30 nm, (b) Si_3N_4/TiO_2 = 20 nm/10 nm, (c) Si_3N_4/TiO_2 = 10 nm/20 nm with L_G = 5 μm, L_{GD} = 5 μm, W_G = 50 μm.

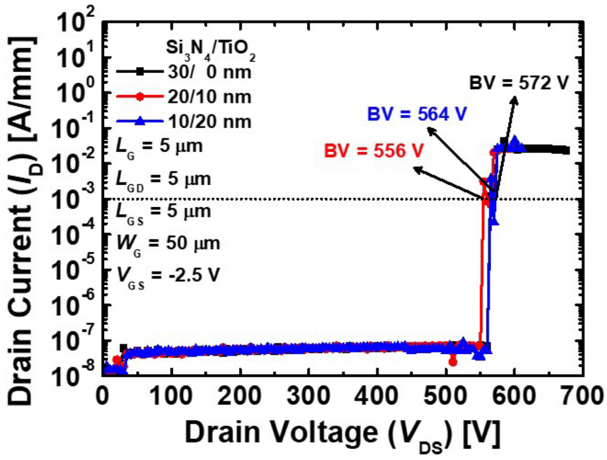
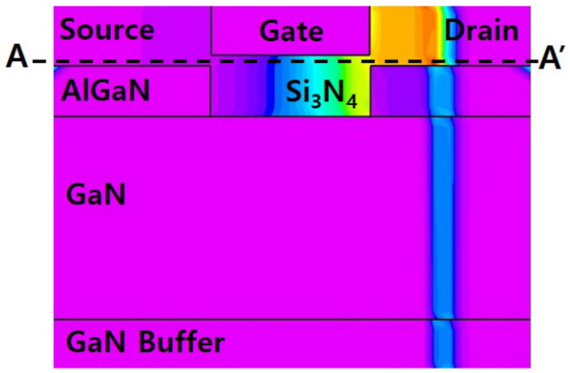


Fig. 6. The BV characteristics of single gate dielectric and dual gate dielectric-based devices with off-state.

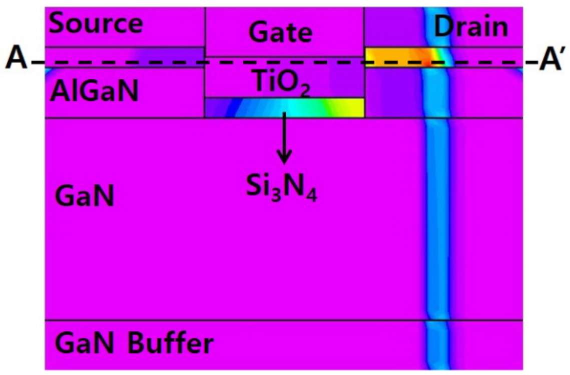
Fig. 5(a)-(c) show the pulsed I−V curves of the single gate dielectric and dual gate dielectric-based devices. Pulsed I−V measurement was performed using the curve tracer B1500A instrument. Gate stress bias V_{GS} = −2 V was applied to completely turn-off the device. Specific on resistances (R_{on}) of the single-gate dielectric (Si_3N_4 = 30 nm), dual-gate dielectric (Si_3N_4/TiO_2 = 20/10 nm), and dual-gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based devices were 116 Ω·mm, 58 Ω·mm, and 43 Ω·mm, respectively. And the $\Delta I_{D,max}$ was 1.64%, 3.5%, and 2.91%, respectively. The $\Delta I_{D,max}$ of the three devices was low due to the MIS structure which improved the gate lag. R_{on} was 62% improvement in the dual gate dielectric-based device with a higher capacitance than a single-gate dielectric-based device, so the performance improvement can be expected in a switching device.

Fig. 6 shows the breakdown voltage (BV) characteristics of the single gate dielectric and dual gate dielectric-based devices with an off-state. BV was extracted at I_D=1 mA/mm. The BV values of single gate dielectric (Si_3N_4 = 30 nm), dual gate dielectric (Si_3N_4/TiO_2 = 20/10 nm), and dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based devices were 572 V, 556 V and 564 V, respectively, with no significant difference because of no change in the structure.

Fig. 7 shows the simulated results of the single gate dielectric (Si_3N_4 = 30 nm) and dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based devices at V_{GS} = −2.5 V and V_{DS} = 500 V. Fig. 7(a) and (b) show the contour map of the electric field distribution of the single gate dielectric (Si_3N_4 = 30 nm) and dual gate dielectric



(a)



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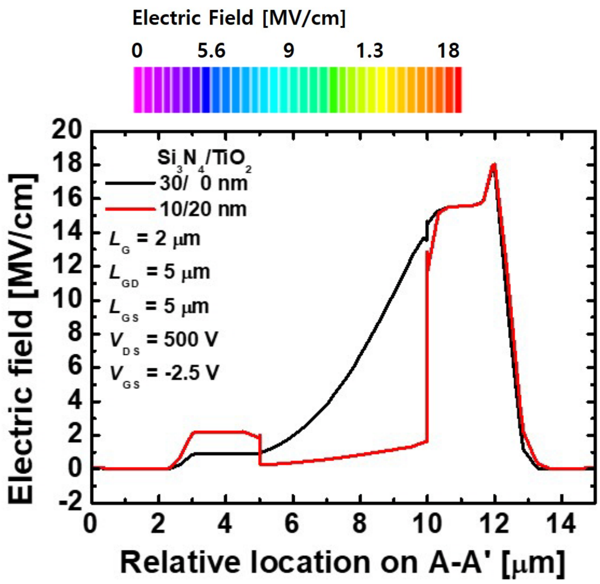

(c)

Fig. 7. The contour map of the electric field distribution of (a) single gate dielectric (Si_3N_4 = 30 nm), (b) dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based devices at V_{GS} = −2.5 V and V_{DS} = 500 V, (c) The Electric field distribution along the A−A′ cut line at the peak electric field strength.

(Si_3N_4/TiO_2 = 10/20 nm)-based devices. Fig. 7(c) shows the electric field distribution along the A−A′ cut line at the peak electric field strength, and the electric fields of single gate dielectric- and dual gate dielectric (Si_3N_4/TiO_2 = 10/20 nm)-based devices were almost similar. BV is greatly affected by the peak electric field with a little change in BV because of a small change in the peak electric field.

IV. CONCLUSION

In this study, we fabricated a recessed gate GaN MOSFET with Si_3N_4/TiO_2 stacked dual gate dielectric and analyzed the DC characteristics. By the gate recess etching on the basic HEMT structure, a normally-off device with a positive V_{th} was fabricated. A dual gate dielectric-based device with a higher oxide capacitance improved the current compared to the single gate dielectric-based device. In addition, it has a great advantage in terms of switching due to relatively low R_{on}. Additionally, it was confirmed that the dual gate dielectric with the thickness of Si_3N_4, is thinner than that of TiO_2, thereby improving the device performance. As a result, the $I_{D,max}$ and g_m of the dual gate dielectric-based device were improved by 292% and 195%, respectively, compared to the single gate dielectric-based device. Moreover, the R_{on} and *SS* were improved by 62% and 68%, respectively. Therefore, the recessed-gate AlGaN/GaN MOSFETs with the stacked Si_3N_4/TiO_2 dual gate dielectric provides a guideline for the power device development research.

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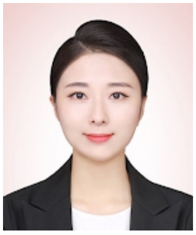

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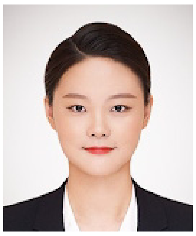

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