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A Review of Noise Reduction Techniques in Noise-shaping SAR ADCs

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***Abstract*—Noise-shaping successive-approximation-register (NS-SAR) ADCs have become one of the most promising candidates for high-resolution data converters over the past decade. This is due to the fact that they combine the advantages of delta-sigma modulation and SAR ADCs. In this hybrid architecture, the quantizer and residue feedback DAC can be replaced by SAR, a replacement which achieves high SNR while also benefiting from superior power efficiency and low cost. For NS-SAR ADCs, various implementations of loop filters for residue processing exist that can realize the noise transfer function (NTF) for NS effects. In addition, many noise reduction techniques have been proposed that suppress additional noises not shaped by NTF. This paper describes the basics of NS-SAR ADCs while also reviewing noise reduction techniques, which include the implementation of a loop filter for residue handling, kT/C noise rejection, and capacitive DAC mismatch error shaping. It also outlines advanced architectures that can overcome the limitations of NS-SAR ADCs.**

***Index Terms*—Analog-to-digital converter, successive approximation register, oversampling, noise shaping, mismatch error shaping**

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I. INTRODUCTION

Modern IoT devices demand high resolution, power efficient ADCs for sensor interfaces such as human body communication, edge computing, and biomedical sensors. Successive approximation register (SAR) ADCs are architectures that are well known for their technology scalability. They are also recognized for their power and area efficiency due to their digitally based building blocks. However, realizing high resolution while maintaining the advantages of SAR ADCs is problematic due to thermal noise such as kT/C and comparator noise. This is because in order to mitigate such noise, the resolution of the CDAC must be increased. Additionally, a low-noise comparator that consumes a lot of power is also required. In the case of CDAC, total capacitance increases exponentially with resolution, which occupies a large area while increasing the power consumption of the driving buffer as well. Given these factors, the benefits of SAR ADCs tend to diminish with increasing resolution.

On the other hand, delta-sigma modulation (DSM) architectures are traditionally regarded as the most promising candidates for high-resolution ADCs due to their oversampling and noise shaping (NS) characteristics. While these noise reduction effects do indeed improve SNR performance by suppressing overall noises, the disadvantage is that DSM architectures require power-hungry op amps, which occupy large areas and cannot easily scale with technology. Furthermore, flash ADC used as a multi-bit quantizer in DSM architectures typically offers lower resolutions, which in turn require a higher oversampling ratio (OSR) to achieve high SNR. It leads to a decrease in power efficiency.

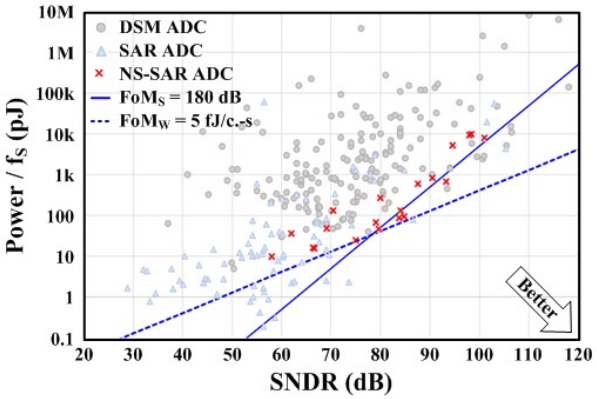

Fig. 1. Power efficiency comparison between NS-SAR ADCs with conventional architectures [42].

Therefore, NS-SAR ADC, a hybrid architecture that combines DSM and SAR ADC to achieve high SNR while maintaining both advantages, has become a promising candidate for high-resolution ADCs in recent years [1-41]. In this hybrid architecture, the SAR ADC is used as a multi-bit quantizer and concurrently as a feedback DAC which processes the residue to achieve noise shaping performance.

Fig. 1 compares the NS-SAR ADCs with conventional SAR and DSM ADCs, which have been published in major conferences [42]. The solid line and dashed line indicate 180 dB of Schreier Figure-of-Merit (FoM_S as shown in Eq. (1)) and 5 fJ/c.-s of Walden FoM (FoM_W as shown in Eq. (2)), respectively. It shows that NS-SAR ADCs are pioneers in terms of power efficiency, as compared with conventional architectures. Reference [36, 37] have reviewed the NS-SAR ADC to show the development of this architecture.

$$FoM_S = SNDR + 10\log\left(\frac{f_B}{power}\right) \tag{1}$$

$$FoM_W = \frac{power}{2^{(SNDR-1.76)/6.02} \times 2 \times f_B} \tag{2}$$

In this paper, the fundamentals of the NS and the advances in noise reduction techniques for NS-SAR ADCs are reviewed. In particular, the loop filter implementations have been described in depth. The rest of this paper is organized as follows. Section II provides the basic concept of NS-SAR ADCs including oversampling and NS mechanisms. Section III outlines the noise reduction techniques employed to realize NS characteristics with residue processing loop filters while Section IV introduces kT/C noise cancellation and CDAC mismatch error shaping (MES). Finally, Section V presents the advanced architectures employed to overcome the limitations of NS-SAR ADCs and Section VI concludes this paper.

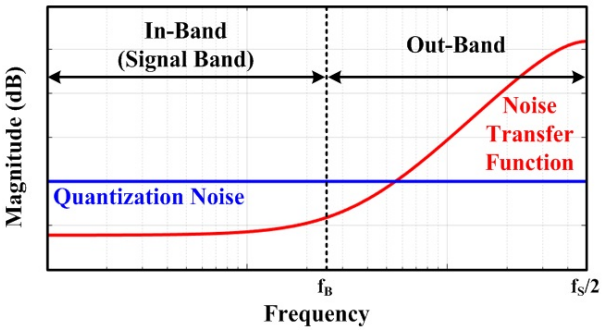

Fig. 2. Quantization noise and noise transfer function (NTF).

II. Basic of Noise-Shaping (NS) SAR ADCs

1. Oversampling

Oversampling is a common method of improving the SNR by reducing quantization noise. The oversampling ADC samples and quantizes the input signal at a much higher sampling rate than the signal band. Therefore, a small fraction of quantization noise falls into the signal band making it possible to filter the out-band noise as shown in Fig. 2. The reduction of quantization noise by oversampling can be quantified as Eq. (3). For better understanding, the signal-to-quantization noise ratio (SQNR) is considered rather than SNR.

$$SQNR = 10\log\left(\frac{P_{signal}}{P_{q,noise}}\right) + 10\log(OSR) \tag{3}$$

where P_{signal} and $P_{q,noise}$ denote signal and quantization noise power, respectively. The OSR is the ratio between the signal band (f_B) and Nyquist range ($f_S/2$). According to the above equation, there is only a 3-dB improvement in SQNR when OSR is doubled. Therefore, a very high OSR is required for high-resolution ADC designs, which has the effect of degrading power

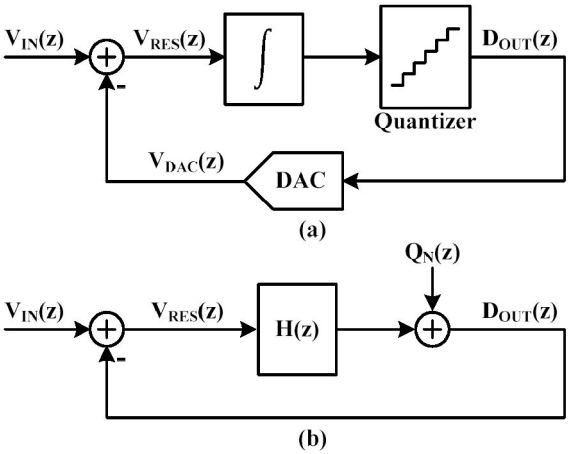

Fig. 3. (a) Block diagram of the 1st-order DSM; (b) signal flow diagram.

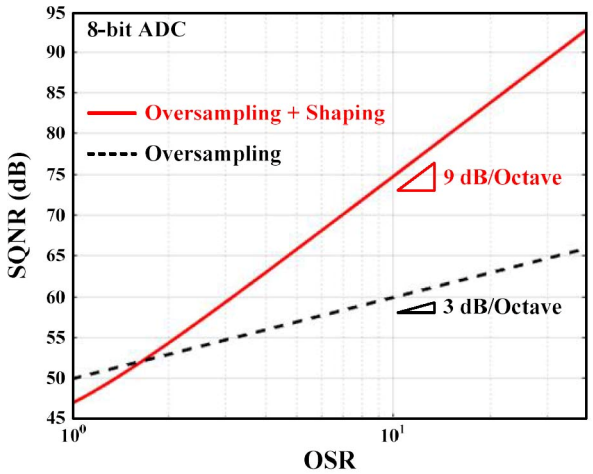

Fig. 4. SQNR improvement by oversampling with and without NS.

efficiency. To overcome this limitation, NS schemes are widely used along with oversampling.

2. Noise Shaping (NS)

Noise shaping is an essential technique and a basic concept of oversampling ADCs to enhance noise reduction effects. This is achieved by attenuating in-band noise through a high-pass noise transfer function (NTF) as shown in Fig. 2. The 1st-order DSM can be an example for presenting the NS mechanism.

The 1st-order DSM consists of a quantizer, a feedback DAC, and an integrator as described in Fig. 3. The quantizer digitizes analog input with feedback DAC converting this digitized data to an analog signal and subtracting from input, making residue voltage that contains quantization noise. Eq. (4) shows a transfer function including quantization noise, $Q(z)$.

$$D_{OUT}(z)=\frac{H(z)}{1+H(z)}V_{IN}(z)+\frac{1}{1+H(z)}Q(z) \quad (4)$$

If the $H(z)$ is a simple discrete-time integrator, $H(z)=z^{-1}/(1-z^{-1})$, then $D_{OUT}(z)$ can be expressed as follows.

$$D_{OUT}(z)=z^{-1}V_{IN}(z)+(1-z^{-1})Q(z) \quad (5)$$

Eq. (5) shows a simple delay signal transfer function (STF), z^{-1}, and a high-pass NTF, $1-z^{-1}$. Therefore, the SQNR including in-band noise attenuation by NTF can be expressed as Eq. (6).

$$SQNR=10\log\left(\frac{P_{signal}}{P_{q,noise}\times IBNG}\right)+10\log(OSR) \quad (6)$$

Note that IBNG denotes in-band noise gain, which is $IBNG=\int_0^{f_B}\left(\left|NTF(f)\right|^2/f_B\right)df$. If NTF is assumed to be $1-z^{-1}$, Eq. (6) can be approximated as follows.

$$SQNR\approx 10\log\left(\frac{P_{signal}}{P_{q,noise}}\right)-10\log\left(\frac{\pi^2}{3}\right)+30\log(OSR) \quad (7)$$

Eq. (7) shows that the SQNR increases 9-dB when OSR is doubled. Fig. 4 compares the SQNR improvement between oversampling with and without NS.

3. Noise-shaping (NS) SAR ADCs

NS-SAR ADCs have been proposed as a means to overcome the shortcomings of DSM ADCs while obtaining similar NS characteristics [1]. The proposed architecture replaces a quantizer and a feedback DAC of CIFF-DSM as a SAR ADC as shown in Fig. 5(a). And it

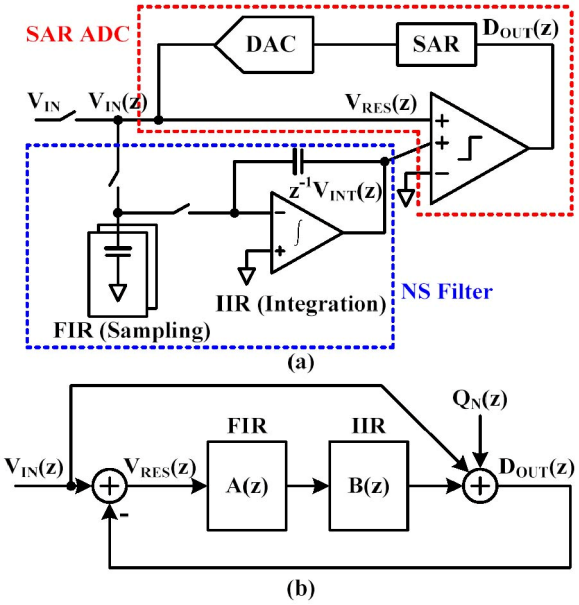

Fig. 5. (a) Block diagram of NS-SAR ADC; (b) signal flow diagram [1].

realizes the NS using a finite-impulse-response and infinite-impulse-response (FIR-IIR) loop filter. The switched-capacitor FIR filter samples the residue and IIR filter integrates this residue. The signal-flow diagram including the FIR-IIR loop filter can be modeled as in Fig. 5(b). Therefore, the overall transfer function is given by Eq. (7).

$$D_{OUT}(z) = V_{IN}(z) + \frac{1}{1 + A(z)B(z)}Q(z) \tag{7}$$

Even though [1] achieves a sharp NTF as shown in Fig. 6, the SNDR is limited due to additional noise generated by the FIR-IIR filter. Furthermore, a power-consuming amplifier is still required. To overcome these limitations, various noise reduction techniques have been proposed. In this paper, the NS-SAR ADCs are classified into active and passive topologies based on the loop filter implementations, which are reviewed in more detail in the following section.

III. Noise Reduction Techniques with Residue Processing

The most important factor of NS-SAR ADCs is how to extract the residue and sum it with the following input

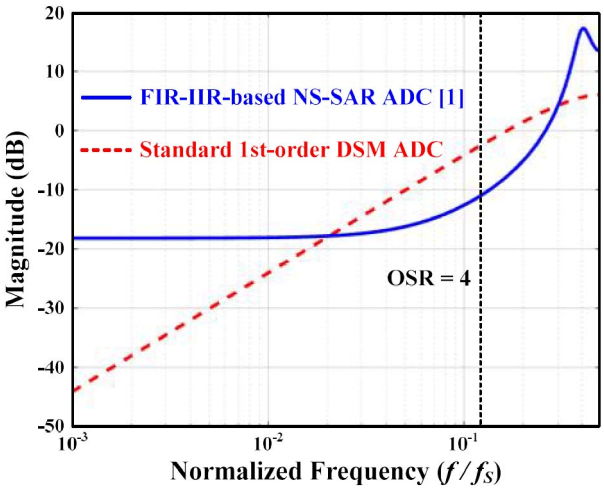

Fig. 6. NTF comparison between NS-SAR [1] and 1st-order DSM ADC.

signal. There are thus two concerns 1) how to process the residue and 2) how to implement the loop filter. With regard to residue processing, both cascaded-integrator-feed-forward (CIFF) and error-feedback (EF) are common implementations. In general, the CIFF structures have a feed-forward path to process the residue and sum it to the following input using a multi-input comparator, whereas the EF structures have a feedback path and sum the residue to the input voltage directly on CDAC. Note that the multi-input comparator introduces extra noise in CIFF and the charge-sharing summation in EF induces signal attenuation.

Fig. 7(a, b) and 8(a, b) shows signal flow diagrams and circuit implementations of CIFF and EF structures, respectively. The corresponding transfer functions are as follows.

$$D_{OUT}(z) = V_{IN}(z) + \frac{1}{1 + H(z)z^{-1}}Q_N(z) \tag{8}$$

$$D_{OUT}(z) = V_{IN}(z) + \left(1 - E(z)z^{-1}\right)Q_N(z) \tag{9}$$

From the circuit implementation of each structure, Eq. (8) and (9) can be translated to Eq. (10) and (11), respectively.

$$D_{OUT}(z) = V_{IN}(z) + \frac{1 - 0.64z^{-1}}{1 + 1.28z^{-1} + 0.64z^{-2}}Q(z) \tag{10}$$

$$D_{OUT}(z) = \frac{14}{16}V_{IN}(z) + \left(1 - \frac{30}{16}z^{-1} + \frac{30}{32}z^{-2}\right)Q(z) \tag{11}$$

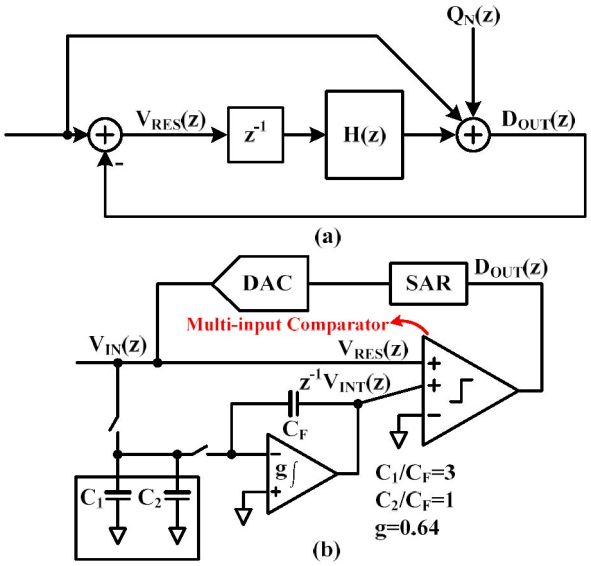

Fig. 7. (a) Signal flow diagram; (b) circuit implementation [1] of CIFF structures.

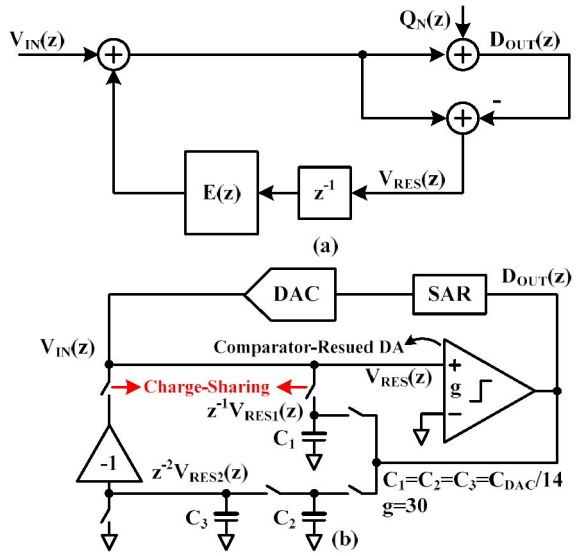

Fig. 8. (a) Signal flow diagram; (b) circuit implementation [13] of EF structures.

Note that, the CIFF structure needs a high-gain integrator to achieve ideal high-pass NTF. On the other hand, the EF structure does not require a high gain integrator but requires a high accuracy opamp. This is because the gain of opamp directly controls the zero of NTF.

Thus, while there are many efforts to alleviate the burden of high gain integrator and multi-input comparator in CIFF structure such as passive integration and capacitor stacking, gain calibrations are introduced to precisely control the gain of opamp in EF structures. Table 1. summarizes and compares the CIFF and EF structures.

Table 1. Comparison between CIFF and EF

Structure	Residue Summation	Gain	Gain Sensitivity	Limitation
CIFF	Multi-input comparator	High	Low	Extra noise
EF	Charge-sharing	Medium	High	Signal attenuation

In terms of loop filter implementation, the loop filter for realizing the NTF of each structure is implemented in two ways, namely active and passive topologies. Generally, an active strategy uses op amps whereas the passive strategy uses simple switches and capacitors to process the residue. More details of these loop filters are provided in the following sections.

1. Active Loop Filter

Active loop filters show flexible and sharp NTF because the amplifier provides sufficient gain. However, the active amplifier consumes large amounts of power which degrades the efficiency of NS-SAR. Therefore, much effort has been expended in a bid to reduce the power consumption of active strategies.

As discussed in the previous section, the first implementation of NS-SAR ADC is an active strategy using the FIR-IIR loop filter proposed in [1]. The switched-capacitor FIR filter and the active-amplifier-based IIR filter samples and integrates the residue, respectively. However, the proposed architecture presents only moderate SNDR performance, even though it has sharp NTF, because the passive residue sampling introduces considerable kT/C noise, with the active amplifier also introducing more noise. Improving noise performance requires the addition of large capacitors for residue sampling, while high-gain, power-consuming amplifiers are required in the IIR filter if the additional noise is to be mitigated.

To relieve the trade-off between kT/C noise and gain loss due to charge sharing in switched-capacitor FIR filter, an input buffer, implemented as an open-loop amplifier between CDAC and residue sampling capacitor, is required [6] as shown in Fig. 9. Although it provides a gain of 2 alleviating kT/C noise in the FIR filter, the

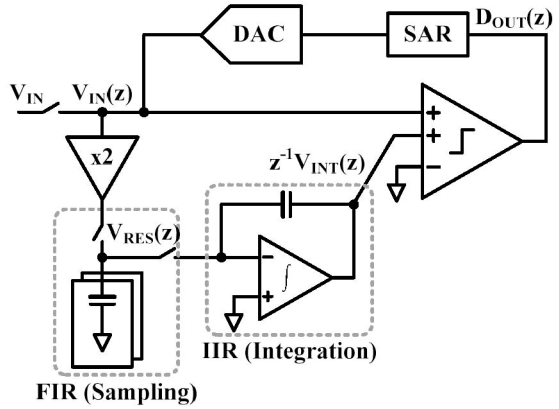

Fig. 9. FIR-IIR loop filter with input buffer [6].

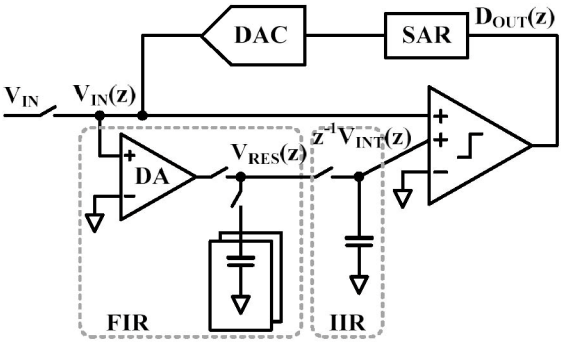

Fig. 10. FIR-IIR loop filter with dynamic amplifier and switched-capacitor implementation [10].

input buffer and active amplifier in the IIR filter together consume 37% of the total power.

In [10, 11], the open-loop dynamic-amplifier-based FIR-IIR filter is proposed as a means of reducing these extra power consumptions. Reference [11] replaces the input buffer and active integrator with low power open-loop dynamic amplifiers and [10] proposes a gain-enhanced dynamic amplifier as the input buffer. Moreover, [10] greatly reduces the residue sampling capacitor, such that the active-amplifier-based IIR filter can be substituted by a simple switched-capacitor integrator as shown in Fig. 10. However, the drawback is that the open-loop dynamic amplifier is sensitive to PVT variation, which degrades the NTF and limits the NS performance. To compensate for this drawback, [13] proposes background calibration for dynamic amplifiers which increases design complexity.

Reference [25] proposes a calibration-free PVT-robust closed-loop 2-stage dynamic amplifier to simplify the design complexity of the calibration as illustrated in Fig. 11. Due to the fact that the gain of the closed-loop

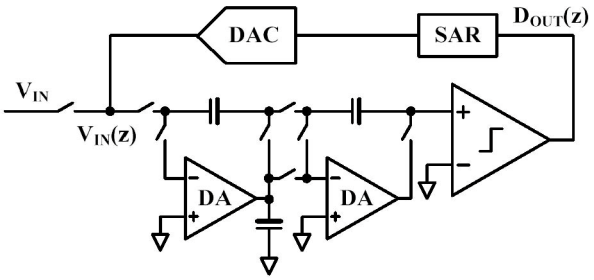

Fig. 11. PVT-robust closed-loop 2-stage dynamic amplifier [25].

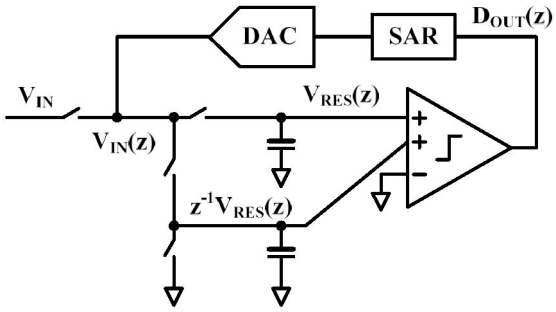

Fig. 12. Fully passive NS-SAR ADC [2].

amplifier is set by capacitor ratios, it is robust in the presence of PVT variations. In [27] and [29], the PVT-insensitive voltage-time-voltage converter and PVT-robust source follower-based unit gain buffer for active residue processing are proposed , respectively.

2. Passive Loop Filter

A passive loop filter is a simple, PVT robust, and scaling-friendly strategy because it consists of switches and capacitors. It is more power-efficient than an active loop filter given that it does not need a power-consuming amplifier. However, the passive strategy suffers from charge sharing in switched-capacitor operation and shows mild NTF due to the insufficient gain. Therefore, many efforts have been expended on reducing the charge sharing and providing adequate gain for the passive loop filter.

The first fully passive NS-SAR ADC is proposed in [2]. The proposed architecture utilizes the switched-capacitor circuit for the purpose of residue sampling and integration. Residue summation is realized by a multi-input comparator as shown in Fig. 12. However, switched-capacitor residue sampling attenuates the input signal by factor of 2 while the charge sharing of residue

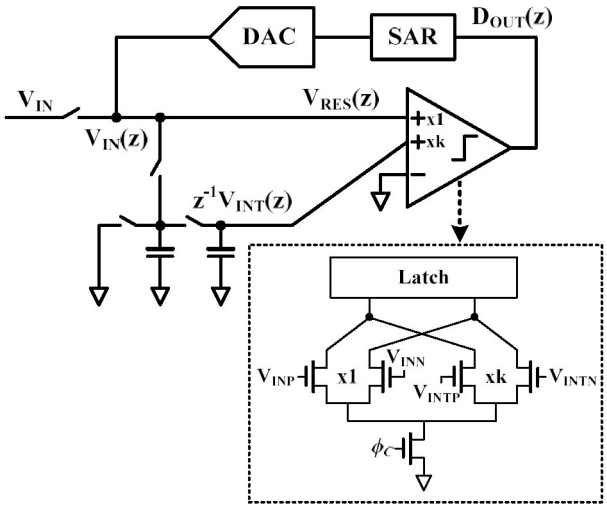

Fig. 13. Passive NS-SAR ADC with relative gain using multi-input comparator [4].

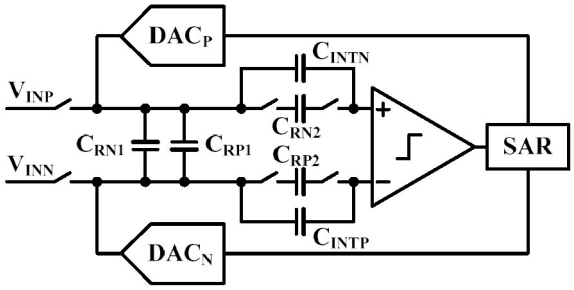

Fig. 14. Passive signal-residue summation with 2x passive gain using capacitor stacking [18].

integration degrades NTF. This architecture is improved in [3] to 2nd-order NS. The 2nd-order NS is realized with the application of capacitor stacking [43] thus achieving passive gain but this does nothing to resolve signal attenuation limitations. Reference [4, 8] eliminates this signal attenuation and realizes sharper NTF than [2, 3]. In addition, the relative gain between input signal and integrated residue is realized through the input transistor sizing of the multi-input comparator as shown in Fig. 13. The multi-input comparator not only provides relative gain but also realizes signal summation. However, the large extra input pair which provides relative gain also introduces additional thermal noise, while the residue sampling and integration introduce extra unshaped kT/C noise, increasing the overall noise.

To alleviate the extra thermal noise from the multi-input comparator, [18] proposes a passive signal-residue summation scheme as shown in Fig. 14. This architecture achieves the residue summation by serialization of

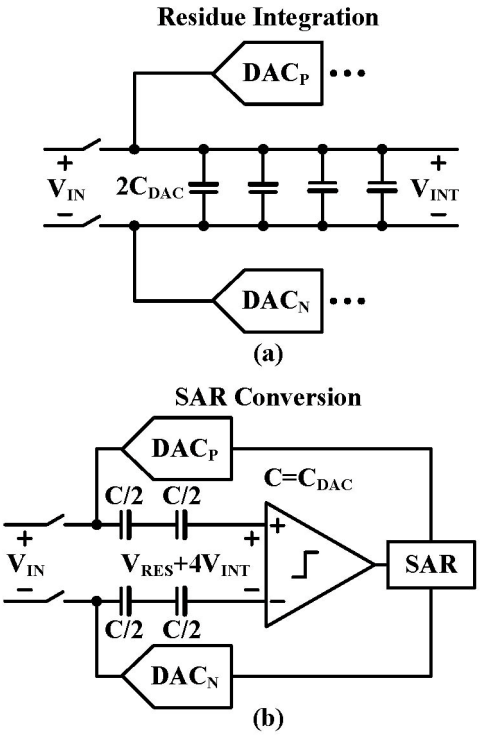

Fig. 15. Passive residue integration with 4x passive gain using capacitor split and stacking [23].

CDAC and integration capacitor. Moreover, the differential residue sampling on back-to-back capacitors provides a passive gain of 2 thereby eliminating the multi-input comparator. Even so, it achieves only 2x passive gain so resulting in mild NTF while the small residue sampling capacitor introduces large kT/C noise.

In [23], the differential integration with split capacitor and capacitor stacking are presented as described in Fig. 15. This scheme eliminates residue sampling and provides 4x the passive gain, which obviates the need for a multi-input comparator. Therefore, it reduces the kT/C and comparator noise significantly. However, it remains difficult to increase gain because the passive gain using capacitor stacking is sensitive to parasitic capacitance.

IV. Additional Noise and Error Reduction Techniques

Although the NTF efficiently suppresses quantization and comparator noise, additional noise and error that are not shaped by NTF remain. These additional non-idealities, such as the CDAC mismatch-induced error and kT/C noise, serve to limit the SNDR of the NS-SAR

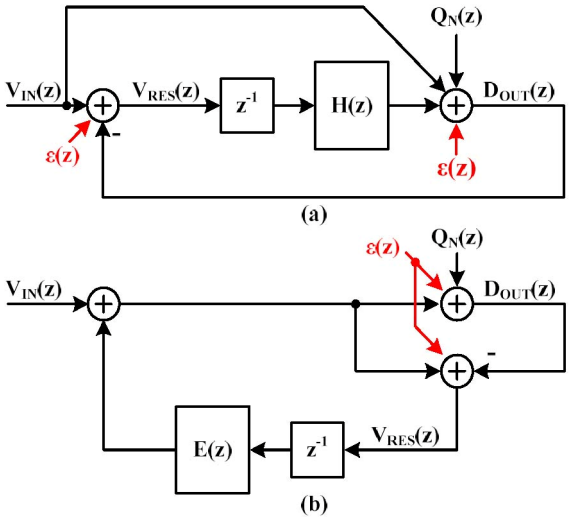

Fig. 16. Signal flow diagram of (a) CIFF; (b) EF structures including noise from CDAC mismatch.

ADCs. This section, therefore, presents the noise and error reduction techniques to mitigate these additional non-idealities.

1. CDAC Mismatch

The CDAC mismatch introduces additional unshaped errors which cause harmonic distortion and increase the in-band noise floor. It can be modeled as an additive noise, ε(z), in a loop filter as shown in Fig. 16. Then $D_{OUT}(z)$ can be expressed as follows.

$$D_{OUT}(z) = V_{IN}(z) + \frac{1}{1+H(z)z^{-1}} Q_N(z) + \varepsilon(z) \quad (10)$$

$$D_{OUT}(z) = V_{IN}(z) + \left(1 - E(z)z^{-1}\right) Q_N(z) + \varepsilon(z) \quad (11)$$

Calibration and mismatch shaping (MS) are commonly used methods to relieve the CDAC mismatch. The first one, calibration, including both the foreground and background method, compensates for CDAC mismatch in the analog and digital domain, and thus it can cancel errors from the CDAC mismatch. Foreground calibration is more widely used than the background method due to the greater simplicity of its implementations. However, foreground calibration needs additional calibration phase interrupting normal operation of ADCs.

The second one, MS suppresses the in-band noise and distortion from CDAC mismatch. The well-known MS

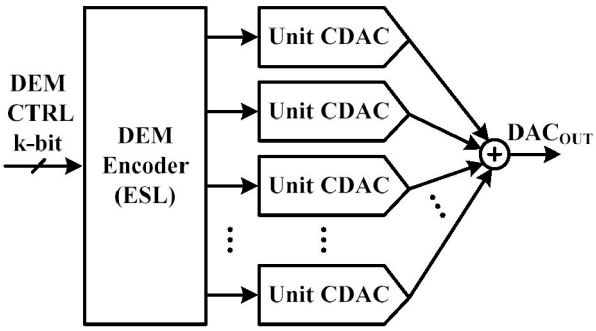

Fig. 17. Block diagram of a simple DEM.

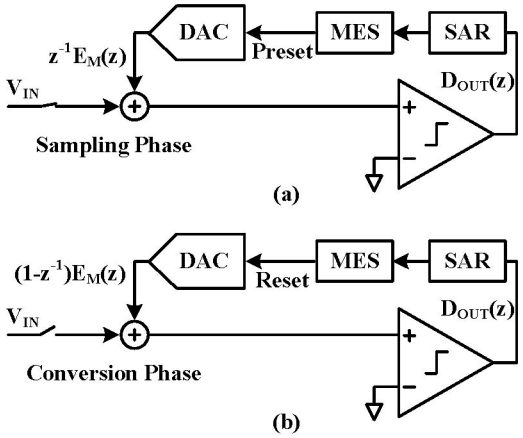

Fig. 18. Block diagram of a simple MES: (a) sampling phase; (b) conversion phase.

are the dynamic elements matching (DEM) [44] and data-weighted averaging (DWA) [45]. An element selection logic (ESL) randomizes and rotates the DAC capacitor as shown in Fig. 17. Therefore, the DEM and DWA suppresses and shapes the in-band harmonic distortion and noise, respectively. The drawbacks of these DEM-based MS methods are complexity and long delay. If higher order shaping is to be achieved, more complicated logic is required, with ESL complexity growing exponentially as CDAC resolution increases. To limit complexity of the ESL, some designs shuffle only a few MSBs, despite the continuing presence of errors from LSBs.

Another MS technique is mismatch error shaping (MES) [6]. Conceptually, it is similar to the NS mechanism. It captures the mismatch error and feeds it back by presetting the LSBs of CDAC before sampling. Fig. 18 illustrates the 1st-order MES operations. During the sampling phase (in Fig. 18(a)), the LSB parts are preset to hold the previous mismatch error, $z^{-1}E_M(z)$.

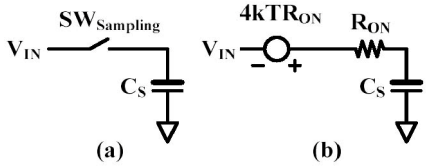

Fig. 19. (a) Simple sampling circuit; (b) its equivalent noise modeling [46].

Following this, the LSB parts are reset in the conversion phase (in Fig. 18(b)) to subtract the previous error from the current error, $E_M(z)-z^{-1}E_M(z)$. Therefore, it realizes a high pass shaping of the CDAC mismatch error, $(1-z^{-1})E_M(z)$. The MES is easier to implement than DEM because it does not require complex logic. However, the MES suffers input dynamic range loss due to LSB presetting.

To alleviate this loss, references [6, 23, 40] apply the DEM or DWA for the MSBs and MES for LSBs. These references can also mitigate the complexity of DEM-based implementations by applying DEM techniques to only some MSBs.

2. kT/C Noise

Sampling kT/C noise is one of the unshaped noises in NS-SAR ADCs. Even though oversampling relieves kT/C noise by OSR, the disadvantage is that increasing OSR limits the signal bandwidth. Fig. 19 shows sampling circuit and its equivalent noise modeling. The on-resistance of the sampling switch introduces the noise power spectral density (PSD) of $4kTR_{ON}$ and its equivalent noise bandwidth (ENBW) is $1/4R_{ON}C_S$. For a simple single-pole system, the total noise power ($\overline{v_n^2}$) can be expressed as the product of the PSD and ENBW [46].

$$\overline{v_n^2} = 4kTR_{ON} \times \frac{1}{4R_{ON}C_S} = \frac{kT}{C_S} \tag{12}$$

Therefore, only the sampling capacitor appears in total noise power. Reference [46, 47] propose a kT/C noise reduction scheme using feedback topology by decoupling the noise PSD and ENBW. Fig. 20(a) and (b) shows a sampling circuit with a single-stage and two-stage

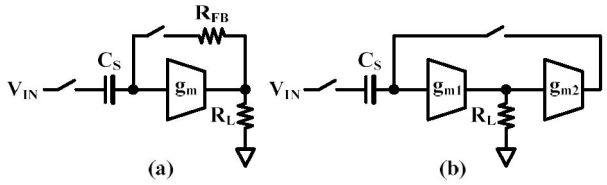

Fig. 20. kT/C noise reduction using feedback topology with (a) single-stage; (b) two-stage amplifier [46, 47].

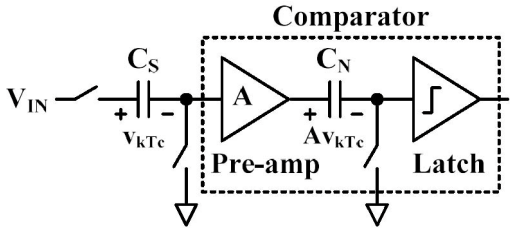

Fig. 21. kT/C noise cancellation using series capacitor [46, 48].

amplifier, respectively. They reduce total sampling noise as follows.

Note that γ is the amplifier noise factor [46, 47].

$$\overline{v_{n1}^2} = \left(\frac{\gamma R_L}{R_L + R_{FB}} + \frac{1}{g_m R_L} + \frac{1}{g_m R_{FB}}\right) \times \frac{kT}{C_S} \tag{13}$$

$$\overline{v_{n2}^2} = \left(\gamma g_{m2} R_L + \frac{g_{m2}}{g_{m1}} + \frac{\gamma}{g_{m1} R_L}\right) \times \frac{kT}{C_S} \tag{14}$$

If the amplifier gain, $g_{m,m1}$ is large, the noises can be approximate as

$$\overline{v_{n1}^2} \approx \frac{\gamma R_L}{R_L + R_{FB}} \times \frac{kT}{C_S} \tag{15}$$

$$\overline{v_{n2}^2} \approx \gamma g_{m2} R_L \times \frac{kT}{C_S} \tag{16}$$

It shows that the sampling noise can be adjusted by R_L, R_{FB}, and g_{m2} while C_S remains constant.

References [22, 30, 46, 48] introduce the active sampling kT/C noise canceling scheme as shown in Fig. 21. This scheme captures the noise on an additional series capacitor (C_N) which is placed between the preamplifier and the latch of the comparator. Then this noise would be canceled in the next phase. Although the additional series capacitor induces extra noise, this is attenuated by preamplifier gain. However, this noise cancellation cannot be employed directly in NS-SAR.

This is because the noise cancellation occurs inside the comparator, which causes the noise captured by C_N to be shaped by NTF. To overcome this limitation, references [22, 30] perform the noise cancellation in the pre-comparator feedback path as shown in Fig. 22. Although EF structure has been adopted to validate the pre-comparator kT/C noise cancellation, they can also be applied to CIFF structures. These techniques alleviate the burden of the ADC input driver by reducing the sampling capacitor.

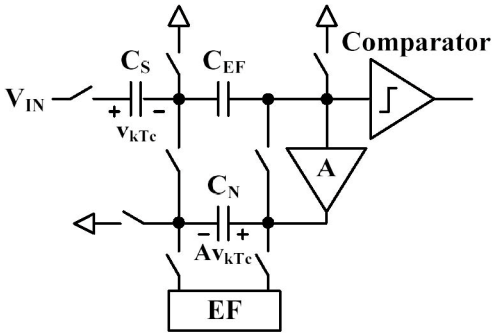

Fig. 22. Pre-comparator kT/C noise cancellation [22, 30].

V. Advanced Architectures (Future Trends)

Even though the NS-SAR ADCs are a high-efficient and low-cost architecture, they still have inherent limitations, such as the challenge of driving large sampling capacitors for high-resolution NS-SAR and limited BW due to the oversampling. This section summarizes the advanced architectures employed in an effort to address these limitations.

1. Hybrid Architectures

In [49], the NS-SAR ADC is employed as a quantizer in continuous time (CT)-DSM ADC so as to achieve a power-efficient 3rd-order NS effect. It is implemented by means of a 1st-order CT-DSM ADC and a fully passive 2nd-order NS-SAR. Thanks to the 2nd-order NS-SAR, the overall loop filter can be simplified given that it needs only a single active amplifier to realize the 3rd-order NS effect.

In [50, 51], the pipelined NS-SAR ADC is proposed to solve BW limitation. The 2nd-stage residue is summed with 1st-stage residue, which amplified by inter-stage residue amplifier. Then further quantized in 2nd-stage, realizing EF NS. Since the 2nd-stage integrates the residue during the 1st-stage sampling and conversion a high-speed pipeline operation is maintained.

In [32, 39], the multi-stage noise-shaping (MASH) ADC is presented. Reference [32] implements NS-SAR assisted pipelined ADC, realizing 2-0 MASH. The 2nd-orer NS-SAR ADC shapes the inter-stage gain error and nonlinearities of pipelined ADC. It relaxes the gain sensitivity of conventional pipelined ADC. Reference [39] proposes 1-1 MASH structure using fully passive

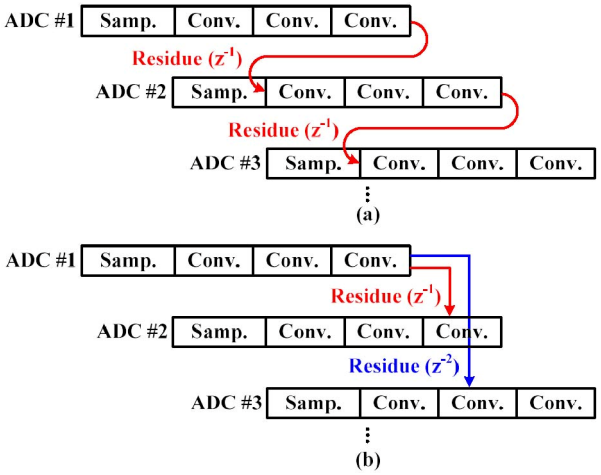

Fig. 23. (a) Inter-channel non-casual feedback; (b) midway feedback proposed in [16].

NS-SAR and VCO ADC alleviating the burden of driving large sampling capacitors. The proposed MASH ADC allows for the use of the low-resolution NS-SAR as a 1st-stage, allowing for small input capacitors while signal attenuation of passive NS-SAR is addressed by leveraging it to linearize the VCO.

2. Time-interleaved Architectures

The oversampling ADCs suffer from the limited BW due to the OSR. Time-interleaved (TI) architecture is a well-known technique for increasing BW. However, this TI strategy is not a straightforward solution for NS-SAR ADCs due to the residue process. Because the multiple channels (sub-ADCs) operate in parallel with overlapping the conversion cycles, the residue from the previous channel cannot be fed back to the adjacent channel directly as shown in Fig. 23(a). To apply the TI technique to NS-SAR ADC, [16] proposes the midway

Table 2. Comparison and summary

Year	Publication	BW (MHz)	Power (μ W)	OSR	NS order	SNDR (dB)	SFDR (dB)	FoM_S (dB)	FoM_W (fJ/c.step)	Structure	Loop Filter	Features
2012	[1] JSSC	11	806	4	1	62.1	72.5	163.5	35	CIFF	Active	First CIFF NS-SAR ADC
2015	[2] VLSIC	6.25	120.7	4	1	58	-	165.2	14.8	EF	Passive	First EF NS-SAR ADC
2016	[3] ASSCC	8	252.9	4	2	64.9	-	169.9	11	EF	Passive	Passive gain with cap. stacking
	[4] ESSCIRC	0.125	61	8	1	74	95	167.1	59.6	CIFF	Passive	Multi-input comp. for relative gain
	[5] VLSIC	0.002	37.1	25	3	98	111.8	175.3	143	CIFF	Active	DEM, modulation dither effect
	[6] JSSC	0.001	15.7	500	1	101	105.1	179	85.6	CIFF	Active	DWA, MES
2017	[7] CICC	1.75	70.5	8	1	68.1	84.8	172	9.7	CIFF	Active	Least squares estimation-based calibration
	[8] VLSIC	0.262	143	16	2	80	-	172.6	33.4	CIFF	Passive	Tri-level majority voting
	[9] VLSIC	25	2400	6	1	69.1	81.2	169.2	20.7	CIFF	Passive	Noise quantizer technique
	[10] ISSCC	5	460	13.2	1	79.7	92.6	180.1	5.8	CIFF	Active	Gain-enhanced dynamic amp.
	[11] CICC	0.25	257.8	20	3	83.4	96.5	173.3	42.6	CIFF	Active	Open-loop integrator, binary DEM
2018	[12] ASSCC	0.05	60	16	2	72	78.7	161.2	184.4	CIFF	Passive	Majority voting, cycle DEM
	[13] ISSCC	0.625	84	8	2	79	89	177.7	9.2	EF	Active	NTF optimization
	[14] MWSCAS	0.002	74.2	32	1	78.8	87.6	153.1	2605.9	EF	Active	2-C DAC
2019	[15] ASSCC	5	108.7	4	2	68.2	84.6	174.8	5.2	CIFF	Active	Optimal 2-zeros & 2-poles, compiled layout
	[16] JSSC	50	13000	4	4	70.4	88	166.3	48	TI-EF	Active	Time-interleaved
	[17] CICC	2	2130	20	2	73.8	87.3	163.5	133	CIFF	Passive	Buffer-embedded
	[18] ISSCC	40	1250	4	1	66.6	77.4	171.6	9	CIFF	Passive	Passive signal-residue summation
	[19] ASSCC	0.625	130	8	2	71	81	167.8	35.9	EF	Active	Dynamic amp., ring amp.
2020	[20] TCAS-I	0.625	70	8	2	74.6	-	174.1	12.8	EF	Active	Configurable band-pass, clock-controlled amp.
	[21] JSSC	0.1	120	10	4	87.6	102.8	176.8	30.6	Cas.-EF	Active	Multi-phase settling amp.
	[23] ISSCC	0.04	67.4	25	1	90.5	102.2	178.2	30.8	CIFF	Passive	Passive gain with cap. stacking, 2^{nd}-order MES
	[24] MWSCAS	0.002	40.8	32	1	82.6	90.9	159.5	925.1	EF	Active	2-C DAC, correlated double sampling
	[25] JSSC	0.625	107	8	2	83.8	94.3	181.5	6.8	CIFF	Active	Closed-loop dynamic amp.
	[26] TCAS-II	3.125	1240	16	2	77	90.1	171	34.3	CIFF	Active	Lossless integrator
2021	[27] ASSCC	0.625	71	8	2	73.8	88.1	173.2	14.2	EF	Active	Open-loop V-T-V converter
	[28] ISSCC	80	2560	4	1	66.3	73.6	171.2	9.5	TI-CIFF	Passive	Coarse-fine segmentation
	[29] ISSCC	0.25	340	10	4	93.3	104.4	182	18	CIFF	Active	Cap. stacking, dynamic buffering
	[30] JSSC	0.625	119	8	3	84.8	103	182	6.7	EF-CIFF	Active	kT/C cancellation, floating inv. dynamic amp.
	[31] JSSC	50	8500	4	2	69.1	-	166.8	36.5	TI-CIFF	Passive	Fully dynamic
	[32] ISSCC	25	1260	8	2	75	92.1	178	5.5	CIFF	Passive	2-0 MASH, NS-SAR assisted pipeline
2022	[33] ISSCC	0.5	133.88	5	4	84.1	97	179.8	10.2	EF-CRFF	Active	EF-cascaded resonator FF, buffer-embedded
	[34] TCAS-II	0.625	113.02	16	2	79.3	90.4	176.7	12	EF	Active	Unity-gain buffer
	[35] JSSC	0.125	96	8	3	79.6	94.8	170.7	49.4	EF-CIFF	Active	Dither-based digital calibration
	[39] JSSC	1.1	160	11	1	71.5	81	169.9	23.7	CIFF	Passive	1-1 MASH using NS-SAR & VCO
	[40] JSSC	5	8006	6	2	84.2	97.3	172.2	60.4	CIFF	Active	Buffer-embedded
	[41] JSSC	0.03125	7.3	16	2	80	98	176.3	14.3	CIFF	Active	Duty-cycled amp. digital-predicted MES

feedback which is multiple feedback to other channels as shown in Fig. 23(b). Thanks to the inherent delay in midway feedback, this allows high-order NTF to be realized. However, as the TI NS-SAR ADC in [16] is implemented on EF architecture, it requires a summing amplifier consuming large static power. Moreover, it shows mild NTF to ensure stability due to the gain of the amplifier being vulnerable to PVT variations. To

overcome these drawbacks of the EF structure, [28, 31] realizes the TI NS-SAR ADC using CIFF architecture. [31] uses the multi-input comparator as a feedforward summation and [28] adopts the passive summation using capacitor stacking scheme. Therefore, the CIFF-based TI NS-SAR ADCs show better power efficiency than EF-based structure due to unnecessariness of a static amplifier.

VI. CONCLUSION

In this paper, the fundamentals of NS-SAR ADCs are described. Additionally, the noise reduction techniques including the implementation of a loop filter, CDAC MES, and kT/C noise cancellation are also reviewed. The loop filters to realize NS effects are categorized as either active or passive topology with the advancements of each topology provided. Additional noise reduction techniques such as CDAC MES and kT/C cancellation to suppress the unshaped noise by NTF are presented. Advanced hybrid architectures capable of overcoming the inherent limitations of NS-SARs are also summarized.

Table 2 compares and summarizes the performance, feedback structure, loop filter implementation, and features of NS-SAR ADCs with chip measurement results.

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REFERENCES

[1] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC," *IEEE Journal of Solid-State Circuits,* vol. 47, no. 12, pp. 2898-2904, 2012.

[2] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 9.35-ENOB, 14.8 fJ/conv.-step Fully-Passive Noise-Shaping SAR ADC," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, 2015, pp. C64-C65.

[3] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 2nd Order Fully-Passive Noise-Shaping SAR ADC with Embedded Passive Gain," in *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2016, pp. 309-312.

[4] W. Guo and N. Sun, "A 12b-ENOB 61μW Noise-Shaping SAR ADC with a Passive Integrator," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, 2016, pp. 405-408.

[5] K. Obata, K. Matsukawa, T. Miki, Y. Tsukamoto, and K. Sushihara, "A 97.99 dB SNDR, 2 kHz BW, 37.1 μW Noise-Shaping SAR ADC with Dynamic Element Matching and Modulation Dither Effect," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2016, pp. 1-2.

[6] Y. S. Shu, L. T. Kuo, and T. Y. Lo, "An Oversampling SAR ADC With DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS," *IEEE Journal of Solid-State Circuits,* vol. 51, no. 12, pp. 2928-2940, 2016.

[7] H. Garvik, C. Wulff, and T. Ytterdal, "An 11.0 bit ENOB, 9.8 fJ/conv.-step Noise-Shaping SAR ADC Calibrated by Least Squares Estimation," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, 2017, pp. 1-4.

[8] W. Guo, H. Zhuang, and N. Sun, "A 13b-ENOB 173dB-FoM 2nd-Order NS SAR ADC with Passive Integrators," in *2017 Symposium on VLSI Circuits*, 2017, pp. C236-C237.

[9] Y. Z. Lin, C. H. Tsai, S. C. Tsou, R. X. Chu, and C. H. Lu, "A 2.4-mW 25-MHz BW 300-MS/s Passive Noise Shaping SAR ADC with Noise Quantizer Technique in 14-nm CMOS," in *2017 Symposium on VLSI Circuits*, 2017, pp. C234-C235.

[10] C. C. Liu and M. C. Huang, "A 0.46mW 5MHz-BW 79.7dB-SNDR Noise-Shaping SAR ADC with Dynamic-Amplifier-based FIR-IIR Filter," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 466-467.

[11] M. Miyahara and A. Matsuzawa, "An 84 dB Dynamic Range 62.5–625 kHz Bandwidth Clock-Scalable Noise-Shaping SAR ADC with Open-Loop Integrator using Dynamic Amplifier," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, 2017, pp. 1-4.

[12] Y. Hwang, Y. Song, J. Park, and D. Jeong, "A 0.6-to-1V 10k-to-100kHz BW 11.7b-ENOB Noise-Shaping SAR ADC for IoT Sensor Applications in 28-nm CMOS," in *2018 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2018, pp. 247-248.

[13] S. Li, B. Qiao, M. Gandara, and N. Sun, "A 13-ENOB 2nd-Order Noise-Shaping SAR ADC Realizing Optimized NTF zeros using an Error-Feedback Structure," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 234-236.

[14] L. Shi, Y. Zhang, Y. Wang, M. Kareppagoudr, M. Sadollahi, and G. C. Temes, "A 13b-ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018, pp. 153-156.

[15] H. Garvik, C. Wulff, and T. Ytterdal, "A 68 dB SNDR Compiled Noise-Shaping SAR ADC With On-Chip CDAC Calibration," in *2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2019, pp. 193-194.

[16] L. Jie, B. Zheng, and M. P. Flynn, "A Calibration-Free Time-Interleaved Fourth-Order Noise-Shaping SAR ADC," *IEEE Journal of Solid-State Circuits,* vol. 54, no. 12, pp. 3386-3395, 2019.

[17] T. Kim and Y. Chae, "A 2MHz BW Buffer-Embedded Noise-Shaping SAR ADC Achieving 73.8dB SNDR and 87.3dB SFDR," in *2019 IEEE Custom Integrated Circuits Conference (CICC)*, 2019, pp. 1-4.

[18] Y. Z. Lin, C. Y. Lin, S. C. Tsou, C. H. Tsai, and C. H. Lu, "20.2 A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC With Passive Signal-Residue Summation in 14nm FinFET," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2019, pp. 330-332.

[19] J. S. Yoon, J. Hong, and J. Kim, "A Digitally-Calibrated 70.98dB-SNDR 625kHz-Bandwidth Temperature-Tolerant 2nd-order Noise-Shaping SAR ADC in 65nm CMOS," in *2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2019, pp. 195-196.

[20] Z. Jiao *et al.*, "A Configurable Noise-Shaping Band-Pass SAR ADC With Two-Stage Clock-Controlled Amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 67, no. 11, pp. 3728-3739, 2020.

[21] L. Jie, B. Zheng, H. W. Chen, and M. P. Flynn, "A Cascaded Noise-Shaping SAR Architecture for Robust Order Extension," *IEEE Journal of Solid-State Circuits,* vol. 55, no. 12, pp. 3236-3247, 2020.

[22] S. Li, "A kT/C-Noise-Cancelled Noise-Shaping SAR ADC with a Duty-Cycled Amplifier," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2020, pp. 758-761.

[23] J. Liu, X. Wang, Z. Gao, M. Zhan, X. Tang, and N. Sun, "A 40kHz-BW 90dB-SNDR Noise-Shaping SAR with 4× Passive Gain and 2nd-Order Mismatch Error Shaping," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 158-160.

[24] L. Shi, E. Thaigarajan, R. Singh, E. Hancioglu, U. K. Moon, and G. Temes, "Noise-Shaping SAR ADC Using a Two-Capacitor Digitally Calibrated DAC with 85.1 dB DR and 91 dB SFDR," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2020, pp. 353-356.

[25] X. Tang *et al.*, "A 13.5-ENOB, 107-μW Noise-Shaping SAR ADC With PVT-Robust Closed-Loop Dynamic Amplifier," *IEEE Journal of Solid-State Circuits,* vol. 55, no. 12, pp. 3248-3259, 2020.

[26] Y. Zhang, S. Liu, B. Tian, Y. Zhu, C. H. Chan, and Z. Zhu, "A 2nd-Order Noise-Shaping SAR ADC With Lossless Dynamic Amplifier Assisted Integrator," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 67, no. 10, pp. 1819-1823, 2020.

[27] C. C. Chen and C. C. Hsieh, "A 12-ENOB Second-Order Noise Shaping SAR ADC with PVT-insensitive Voltage-Time-Voltage Converter," in *2021 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2021, pp. 1-3.

[28] C. Y. Lin, Y. Z. Lin, C. H. Tsai, and C. H. Lu, "An 80MHz-BW 640MS/s Time-Interleaved Passive Noise-Shaping SAR ADC in 22nm FDSOI Process," in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, vol. 64, pp. 378-380.

[29] J. Liu, D. Li, Y. Zhong, X. Tang, and N. Sun, "A 250kHz-BW 93dB-SNDR 4th-Order Noise-Shaping SAR Using Capacitor Stacking and

Dynamic Buffering," in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, vol. 64, pp. 369-371.

[30] T. H. Wang, R. Wu, V. Gupta, X. Tang, and S. Li, "A 13.8-ENOB Fully Dynamic Third-Order Noise-Shaping SAR ADC in a Single-Amplifier EF-CIFF Structure With Hardware-Reusing kT/C Noise Cancellation," *IEEE Journal of Solid-State Circuits,* vol. 56, no. 12, pp. 3668-3680, 2021.

[31] H. Zhuang, J. Liu, H. Tang, X. Peng, and N. Sun, "A Fully Dynamic Low-Power Wideband Time-Interleaved Noise-Shaping SAR ADC," *IEEE Journal of Solid-State Circuits,* vol. 56, no. 9, pp. 2680-2690, 2021.

[32] H. Zhang, Y. Zhu, C. H. Chan, and R. P. Martins, "A 25MHz-BW 75dB-SNDR Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC with Background Offset Calibration," in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, vol. 64, pp. 380-382.

[33] T. Wang, T. Xie, Z. Liu, and S. Li, "An 84dB-SNDR Low-OSR 4th-Order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, 2022, vol. 65, pp. 418-420.

[34] P. Yi, Y. Liang, S. Liu, N. Xu, L. Fang, and Y. Hao, "A 625kHz-BW, 79.3dB-SNDR Second-Order Noise-Shaping SAR ADC Using High-Efficiency Error-Feedback Structure," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 69, no. 3, pp. 859-863, 2022.

[35] Q. Zhang *et al.*, "A 13-Bit ENOB Third-Order Noise-Shaping SAR ADC Employing Hybrid Error Control Structure and LMS-Based Foreground Digital Calibration," *IEEE Journal of Solid-State Circuits,* pp. 1-1, 2022.

[36] L. Jie *et al.*, "An Overview of Noise-Shaping SAR ADC: From Fundamentals to the Frontier," *IEEE Open Journal of the Solid-State Circuits Society,* vol. 1, pp. 149-161, 2021.

[37] G. M. Salgado, D. O'Hare, and I. O'Connell, "Recent Advances and Trends in Noise Shaping SAR ADCs," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 68, no. 2, pp. 545-549, 2021.

[38] L. Shen, Z. Gao, X. Yang, W. Shi, and N. Sun, "A 79dB-SNDR 167dB-FoM Bandpass ΔΣ ADC Combining N-Path Filter with Noise-Shaping SAR," in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, vol. 64, pp. 382-384.

[39] S. T. Chandrasekaran, S. P. Bhanushali, S. Pietri, and A. Sanyal, "OTA-Free 1–1 MASH ADC Using Fully Passive Noise-Shaping SAR & VCO ADC," *IEEE Journal of Solid-State Circuits,* vol. 57, no. 4, pp. 1100-1111, 2022.

[40] Y. Guo, J. Jin, X. Liu, and J. Zhou, "A 60-MS/s 5-MHz BW Noise-Shaping SAR ADC With Integrated Input Buffer Achieving 84.2-dB SNDR and 97.3-dB SFDR Using Dynamic Level-Shifting and ISI-Error Correction," *IEEE Journal of Solid-State Circuits,* pp. 1-12, 2022.

[41] H. Li, Y. Shen, H. Xin, E. Cantatore, and P. Harpe, "A 7.3-uW 13-ENOB 98-dB SFDR Noise-Shaping SAR ADC With Duty-Cycled Amplifier and Mismatch Error Shaping," *IEEE Journal of Solid-State Circuits,* vol. 57, no. 7, pp. 2078-2089, 2022.

[42] B. Murmann, "ADC Performance Survey 1997-2022," *https://web.stanford.edu/~murmann/adcsurvey.html,* 2022.

[43] I. Ahmed, J. Mulder, and D. A. Johns, "A Low-Power Capacitive Charge Pump Based Pipelined ADC," *IEEE Journal of Solid-State Circuits,* vol. 45, no. 5, pp. 1016-1027, 2010.

[44] R. J. V. D. Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," *IEEE Journal of Solid-State Circuits,* vol. 11, no. 6, pp. 795-800, 1976.

[45] R. T. Baird and T. S. Fiez, "Linearity Enhancement of Multibit Delta Sigma A/D and D/A Converters using Data Weighted Averaging," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 42, no. 12, pp. 753-762, 1995.

[46] R. Kapusta, H. Zhu, and C. Lyden, "Sampling Circuits That Break the kT/C Thermal Noise Limit," *IEEE Journal of Solid-State Circuits,* vol. 49, no. 8, pp. 1694-1701, 2014.

[47] Z. Li *et al.*, "A SAR ADC with Reduced kT/C Noise by Decoupling Noise PSD and BW," in *2020 IEEE Symposium on VLSI Circuits*, 2020, pp. 1-2.

[48] J. Liu, X. Tang, W. Zhao, L. Shen, and N. Sun, "A

13-bit 0.005-mm2 40-MS/s SAR ADC With kT/C Noise Cancellation," *IEEE Journal of Solid-State Circuits,* vol. 55, no. 12, pp. 3260-3270, 2020.

[49] J. Liu, S. Li, W. Guo, G. Wen, and N. Sun, "A 0.029mm2 17-FJ/Conv.-Step CT Delta-Sigma ADC with 2nd-Order Noise-Shaping SAR Quantizer," in *2018 IEEE Symposium on VLSI Circuits*, 2018, pp. 201-202.

[50] Y. Song, Y. Zhu, C. Chan, L. Geng, and R. P. Martins, "A 77dB SNDR 12.5MHz Bandwidth 0-1 MASH $\Sigma\Delta$ ADC Based on the Pipelined-SAR Structure," in *2018 IEEE Symposium on VLSI Circuits*, 2018, pp. 203-204.

[51] Y. Song, Y. Zhu, C. H. Chan, and R. P. Martins, "A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, 2020, pp. 164-166.

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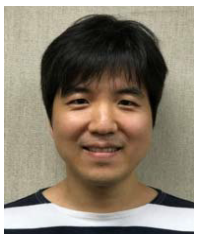

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