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Multi-gate BCAT Structure and Select Word-line Driver in DRAM for Reduction of GIDL

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Abstract—**In this article, we evaluate gate induced drain leakage that affects the refresh time of buried cell array transistor DRAM cells. We proposed a multi-gate BCAT structure to minimize gate induced drain leakage and modified the select word-line circuit to operate multi-gate buried cell array transistor by adding only one PMOS. In the multi-gate structure, by changing the gate voltage, the work function of the metal gate was adjusted to effectively mitigate the electric field formed in the drain region by approximately four orders. As an adopting multi-gate structure, band to band tunneling is suppressed and gate induced drain leakage current is reduced. We verified that the dual-gate structure had less leakage current than the poly-Si BCAT using the TCAD simulation. The reduction of leakage according to the number of gates is inferred by confirming the reduction in GIDL of the three-gate structure compared with the dual-gate structure. Furthermore, the SPICE simulation confirmed that the proposed select word-line circuit transmits different optimized voltages to multiple gates when it is off than while transferring the same voltage when on. This structure can also be extended for application to other DRAM structures, such as the vertical structure and 3D-stacked DRAMs.**

Index Terms—**Refresh time, gate induced drain leakage (GIDL), buried cell array transistor (BCAT), select word-line driver (SWD)**

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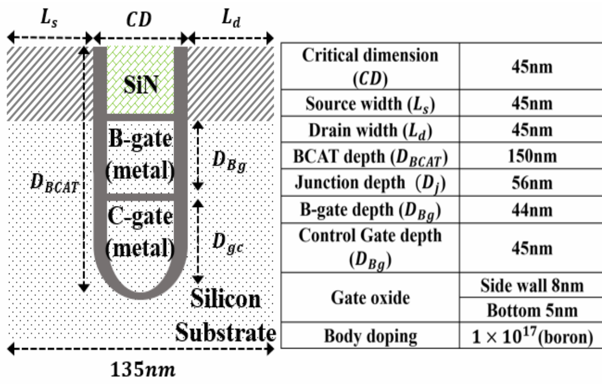
I. INTRODUCTION

Dynamic random access memory (DRAM), which is used as a main memory device, comprises a capacitor and an access transistor. As big data advances, demands for high-storage capacity and high-performance memory in DRAM has increased. Consequently, DRAM manufacturing process technology has achieved high density, enabling high-performance and high-storage capacity DRAM [1]. However, in the process of scaling-down, the short channel effect (SCE) is caused by a decrease in the channel length [2, 3]. SCE results in poorer performance and reliability issues in DRAM because of an increase in the leakage current. To solve this problem, the cell transistor is developed from the planar to a buried cell array transistor (BCAT) structure, which has a buried gate for suppressing the leakage current by extending the effective channel length [4-7]. Punch through and DIBL were suppressed using the BCAT structure, but the gate induced drain leakage (GIDL) was not. GIDL is a tunneling effect that occurs mainly in regions where the drain and gate overlap. It occurs when the band gap is thinned owing to an abrupt voltage difference between the drain and the gate in the off state. The oxide thickness has been continuously decreasing due to scaling, it can easily lead to GIDLs. Therefore, the DRAM performance, especially refresh time (T_{ref}) [8], is significantly influenced by GIDL [9]. To prevent tunneling, it is important to reduce the electric field formed in the drain region.

In this study, we propose a multi gate BCAT structure and modified SWD circuit to suppress GIDL. The dual-gate BCAT, which is a type of multi-gate BCATs, has two metal gates placed up and down. The upper gate,



Critical dimension (CD)	45nm
Source width (L_s)	45nm
Drain width (L_d)	45nm
BCAT depth (D_{BCAT})	150nm
Junction depth (D_j)	56nm
B-gate depth (D_{Bg})	44nm
Control Gate depth (D_{Bg})	45nm
Gate oxide	Side wall 8nm
	Bottom 5nm
Body doping	1×10^{17}(boron)

Fig. 1. 2-D view of dual-gate BCAT structure.

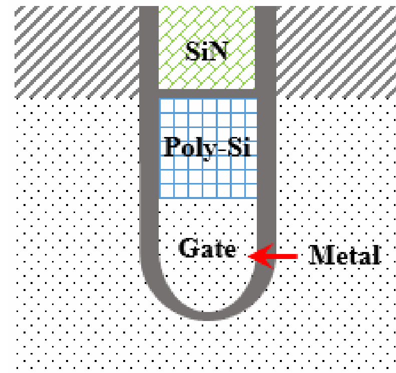


Fig. 2. 2-D view of Poly-Si BCAT structure.

referred to as the bump gate (B-gate), adjusts the work-function (WF) of the gate by applying an appropriate voltage that is different from the lower gate [10]; therefore, the electric field formed in the drain region is alleviated. To operate the dual-gate BCAT, two SWD circuits are required that apply different voltages to the two gates. Here, we present a circuit that operates by adding only one PMOS to the conventional SWD circuit.

The multi-gate BCAT structure and proposed SWD circuit were verified using TCAD and SPICE simulations.

II. Device Structure and Simulation Setup

A simulation was performed considering the terminologies and parameters of the BCAT structure at the 1y-nm technology nodes.

The depth of the gate trench was 150 nm, the gate oxide thickness along the sidewall of the trench was 8 nm, and the bottom of the trench was 5 nm. The drain/source doping depth was 56 nm. To evaluate the GIDL, we applied 4 V to the drain and -2 V~2 V to the lower gate, which is more severe than the actual DRAM operating conditions. In the TCAD device simulations, we incorporated the following models: 1) doping dependent Shockley-Read-Hall recombination; 2) band-to-band tunneling (BTBT), 3) and continuously variable transmission (CVT).

III. BCAT Structure

The most important aspect of reducing the GIDL is to suppress the electric field in the drain region [11]. When

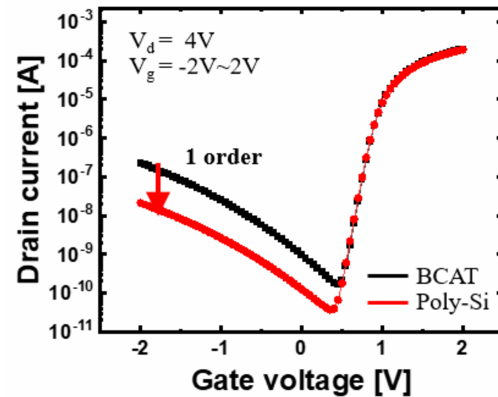


Fig. 3. I-V characteristic comparison between BCAT and Poly-Si BCAT.

turned off, a positive voltage is applied to the drain, and a negative voltage is applied to the gate. Therefore, the electric field formed in the drain region becomes stronger, especially between the drain region and the gate. This electric field can be reduced in the developed BCAT structure by using poly-Si, as shown in Fig. 2, 3 The poly-Si structure can alleviate the abrupt WF difference between the gate and the drain by placing the doped poly-Si on the gate. By adjusting the silicon's WF to an appropriate value, the electric field of the drain region is decreased, and the GIDL is also reduced alongside the electric field. Fig. 5 showed that the WF of silicon was optimized around 4.0 eV. The WF of silicon is determined by the doping concentration, but theoretically, the reachable WF of silicon is 4.05 eV. Additionally, owing to the out dopant diffusion occurring in the fabrication process [12], the WF of silicon is significantly different from the optimized value. Therefore, optimization is impossible in a BCAT structure using doped poly-Si.

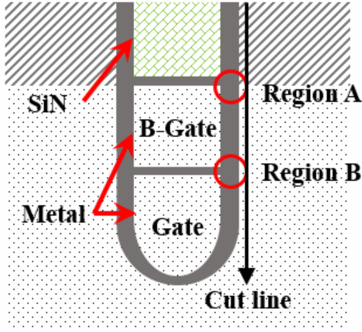


Fig. 4. GIDL generation region of BCAT structure.

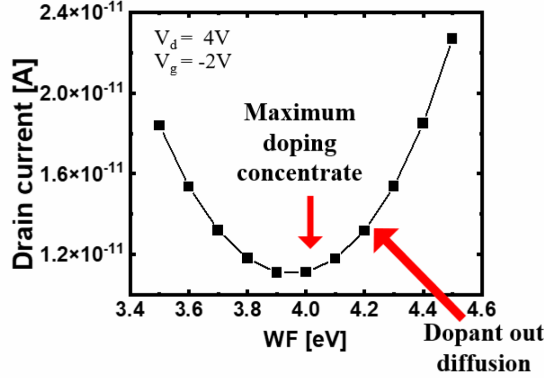


Fig. 5. Results showing the optimization and actual reachable values when adjusting the WF of Poly-si in the off state (V_g = -2 V and V_d = 2 V).

IV. Proposed Multi-gate Structure

1. Dual-gate BCAT Structure

As can be observed from the simulation of poly-Si BCAT, to effectively alleviate GIDL, a material with a WF value of approximately 4.0 is necessary between the gate and the drain. Therefore, another material is needed to overcome the limitations of the WF range of silicon. Fig. 1 shows the proposed dual-gate BCAT structure, which is a type of multi-gate BCAT. In this structure, the electric field is reduced by the B-gate instead of the doped poly-Si. The BTBT current can be expressed as (1)

$$I_{BTBT} = A \times w \times \frac{E_S}{B} \exp\left(\frac{B}{E_S}\right) \quad (1)$$

B : tunneling constant
A : constant depletion depth
W : width of the device
$\boldsymbol{E_s}$: large electric field

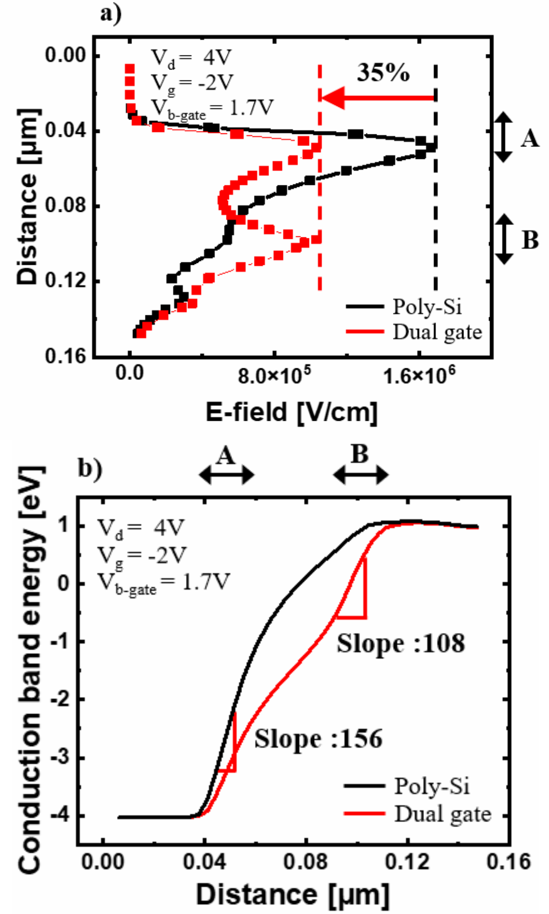


Fig. 6. The simulation result of GIDL in dual-gate BCAT structure: (a) E-field plot along the cut line in the drain region compared to Poly-Si; (b) Conduction band energy plot along the cut line in the drain region compared to Poly-Si.

To minimize the leakage current, the electric field formed in the A and B regions should be made uniform so that any one region is not excessive. To achieve this, it is necessary to adjust the WF by applying an appropriate voltage to the B-gate. We proceeded with the optimization by changing the voltage of the B-gate in the presented simulation environment. Fig. 6(a) shows the electric field changes in regions A and B when an optimized voltage was applied, compared with poly-Si BCAT. Fig. 7 shows the GIDL current according to the voltage. As shown in the graph presented, when a voltage of approximately 1.7 V at the B-gate is applied in a given environment, it was confirmed that the electric field is uniformly distributed to regions A and B, and the GIDL current is minimized. The optimized values are reduced by approximately four orders compared with the conventional values.

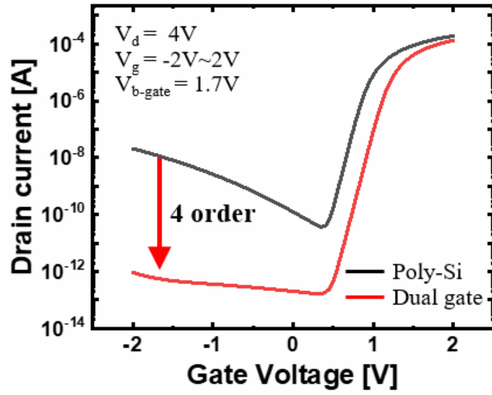


Fig. 7. I-V characteristic of dual-gate BCAT and Poly-Si BCAT.

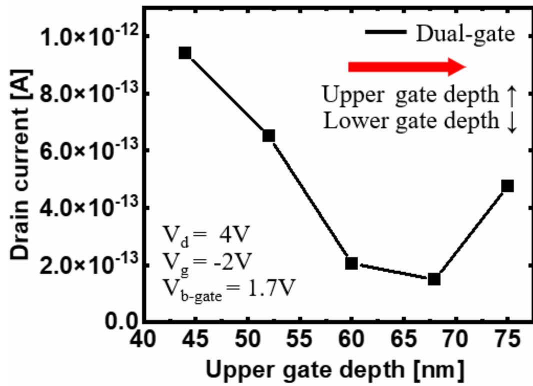


Fig. 8. Drain Current graph with off according to depth change in upper gate.

And we also optimized by changing the upper gate and depth in dual-gate structure from 44 nm to 75 nm. As a result, there was no significant difference as the optimization voltage Therefore, the same 1.7 V was applied regardless of the change in the gate length. However, when the ratio of the lower gate is decreased, it may be seen that the GIDL value increases. Conversely, if the upper gate(B-gate) is increased, the GIDL decreases, and from about upper gate length of 68 nm, the region where the GIDL occurs dominantly changes from A to B, and at this time, it is confirmed that the drain current of off state increases again. Fig. 8 shows the result of the gate length change. however, an upper gate length of 44 nm, top-bottom ratio of 5:5 was selected for the simulation to be applied to all cell transistors in the simulation. This is because when the gate area decreases, the sheet resistance increases, and a voltage cannot be properly applied to all DRAM transistors.

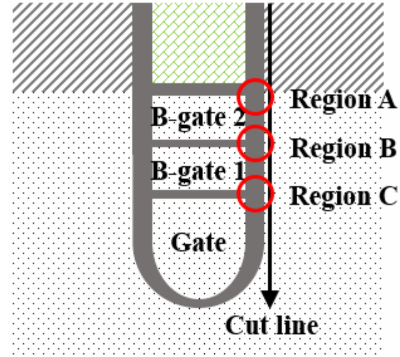


Fig. 9. 2-D view of three-gate BCAT structure.

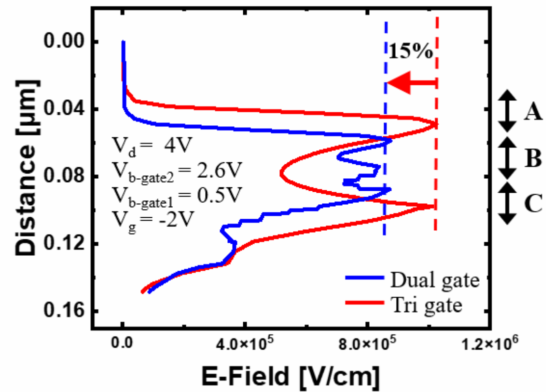


Fig. 10. The simulation result of three-gate BCAT in off state. E-field plot along the cut line in the drain region compared to dual-gate BCAT.

2. Three-gate BCAT Structure

We conducted a simulation by changing the number of gates to determine the effect of gate numbers on GIDL mitigation. In the three-gate BCAT structure shown in Fig. 9 strong electric fields were formed in regions A, B, and C and the electric fields were uniformly distributed like in the dual gate structure. The structure was optimized by applying a voltage of 0.5 V to B-gate1 and 2.6 V to B-gate2. Fig. 11 shows that the GIDL of the three-gate was reduced by approximately two orders compared with the dual-gate structure. It was confirmed that the larger the number of gates, the better the GIDL.

V. SWD CIRCUIT

In this study, we evaluate the GIDL current in the DRAM cell transistor. The structure has two metal gates which are arranged vertically and reduce GIDL by applying different voltages to the gates. Applying an

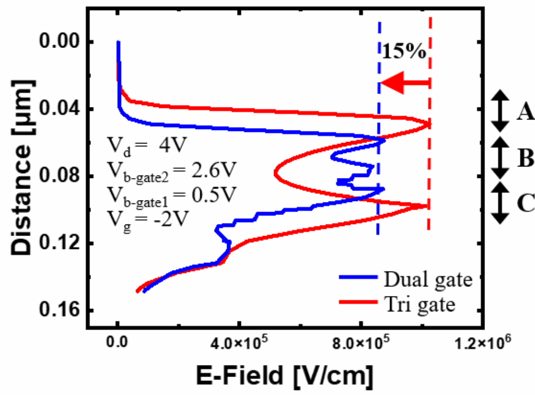


Fig. 11. Simulation results from 3-gate BCAT in off state.

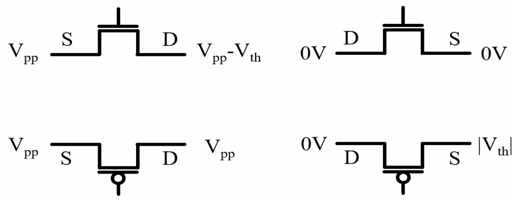


Fig. 12. Configuration of NMOS and PMOS pass transistors.

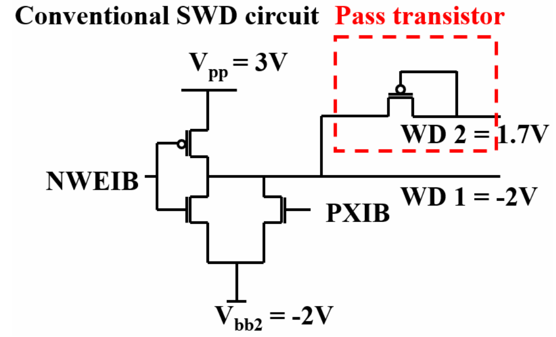


Fig. 13. The modified select-word line driver circuit diagram.

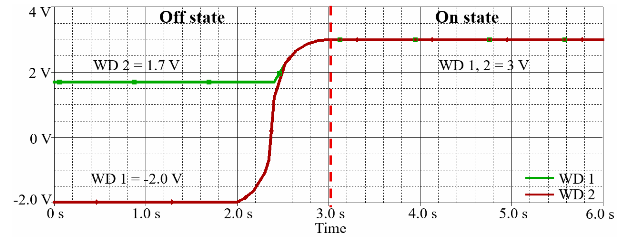


Fig. 14. Output characteristic of SWD circuit as shown in Fig. 12.

optimized voltage to the upper gate alleviates the electric field that causes tunneling between the drain and the gate. In the TCAD simulation, GIDL was reduced by approximately four orders in the proposed structure compared with the poly-Si BCAT structure. To operate the proposed BCAT structure, we modified the conventional SWD circuit by adding one pass transistor. The pass transistor transmits an input signal to the output node, when the gate is turned on, and to enter the high Z state when the gate is off to maintain the previous state. However, there is a problem in transmitting voltage. A pass transistor using NMOS has no problem in transmitting 0 V (low), but if V_{dd} (high) is applied to an input node (drain), the output node (source) voltage gradually increases, and if $V_{gs}<V_{th}$, the device shuts off. Thus, the output voltage becomes V_{dd}-V_{th}. In contrast, PMOS has no problem in transmitting V_{dd}, but the lowest voltage that the output node can reach is $|V_{th}|$. Fig. 12 shows the configuration and output according to the input of the NMOS and PMOS pass transistors, and at this time, both gates are applied with Vdd. Fig. 13. Fig. 14 shows the operation of the proposed SWD circuit, in which different voltages are supplied depending on the Vth of the pass transistor in the off state and the same voltage is supplied in the on state.

The conventional SWD circuit consists of one PMOS and two NMOSs. When in the on state, the NWEIB and PXIB are in the low, and the PMOS connected to the V_{pp} is turned on and the V_{pp} is delivered to the WD. Conversely, when it is off, NWEIB and PXIB become high, and the NMOS connected to V_{bb2} is turned on, and V_{bb2} is delivered to WD.

In order to operate the proposed scheme, it is important to apply the same V_{dd} voltage in the on state and to apply the different optimized voltage to each gate in the off state. Therefore, we propose a new SWD circuit.

We constructed a new circuit that adds a pass transistor using PMOS to the conventional SWD circuit. The circuit transmits the same V_{pp} voltage to WD1 and WD2 in the on state. In the off state, V_{bb2} is transmitted to WD1, but a V_{bb2}+V_{th} voltage is applied to WD2 while passing through the pass transistor.

Additionally, the effect of the number of gates on GIDL was evaluated. As the number of gates increased, GIDL decreased. However, owing to the decrease in the area of the gate, the resistance of the word-line increases; thus, a close additional review is required before use in an actual process. Finally, the multi-gate BCAT structure and modified circuit are compatible with the existing CMOS process and are also available for 3D stacked and vertical DRAM.

VI. CONCLUSIONS

In this study, we evaluate the GIDL current in the DRAM cell transistor. A multi-gate BCAT structure was proposed to minimize the GIDL current. The multi-gate BCAT is a structure in which two metal gates are placed, which reduces the GIDL by applying different voltages to the gates. Applying an optimized voltage to the upper gate alleviates the electric field that causes tunneling between the drain and the gate. In the TCAD simulation, GIDL was reduced by approximately four orders in the proposed structure compared with the poly-Si BCAT structure. To operate the proposed BCAT structure, we modified the existing SWD circuit by adding one transistor.

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