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Low Power RF Interface of the Near-field Communications Tag IC for Sensors

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Abstract—**In this paper, we propose the RF interface of NFC tag IC which is necessary for transmitting the results obtained using blood glucose sensor, water quality sensor, gas sensor and radioactive sensor to portable devices such as mobile phones. The proposed RF interface complies with the ISO14443 type-A standard using 100% ASK and solves the power and clock generation difficulties by using the internal V_{TH} canceling rectifier that is based on the high efficiency voltage doubler and the switching phase locked loop. In the measurement results, the internal V_{TH} canceling rectifier in the RF interface shows more than 80% power efficiency from 100% ASK signal, and successfully generates 1.8 V / 2.5 V supply from the input signal power higher than 6 dBm through low loss voltage regulator. Additionally, we can verify that the proposed switching phase locked loop is locked at 8 dBm or higher input signal power and successfully demodulates ASK input signal.**

Index Terms—**Near-field communication, RFID, tag IC, voltage doubler, phase-locked loop, passive transponder**

I. INTRODUCTION

While RFID technology is widely distributed recently, it has been utilized in a wide range of area such as management of logistics and supply chain, portable health care unit, contactless payment system, on-board biomedical system in the human body, and architecture access control system etc. The design of low-cost transponder is required for the management of logistics and supply chain while miniaturization is essential for insertion into the human body in the case of biomedical system. For a passive transponder, there are difficulties that not only working area is limited but also it has to be satisfied with both low power consumption and secure of operating area at once since it operates without battery [6]. Passive transponders can operate at LF band (135 kHz), HF band (13.56 MHz), UHF band (860~960 MHz) and microwave band (~2.45 GHz). For LF and HF band of them, it can work through inductive coupling in the near magnetic field while it work based on a long distance electromagnetic wave for UHF and microwave band. Communications between readers and transponders are divided into uplink and downlink. Transponders generate and transmit the modulated signal in the downlink while it executes load modulation (LF, HF) or backscatter modulation (UHF) in the uplink. Since the power generation is not easy in downlink and thus the transmission distance is limited, the rectifiers based on voltage doubler are generally used to overcome this. Also, it's desirable to use RF clamps (RF limiter) to protect the transponder from overvoltage situation in the strong filed. According to ISO14443 standard, for type-A, readers use 100% ASK modulation system to commute with transponders [1-3] while 10% ASK modulation is used

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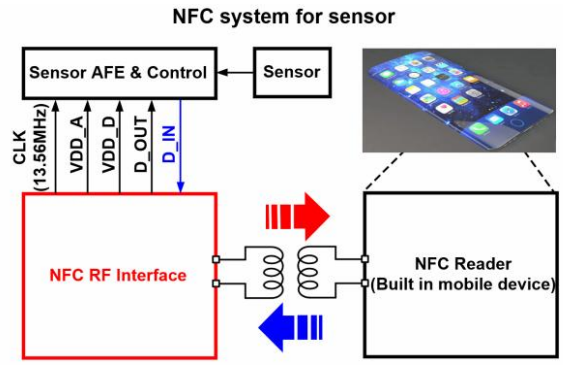

Fig. 1. The block diagram of the near field communication system for sensors.

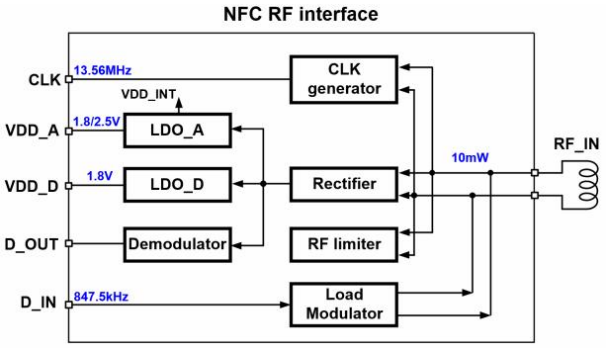

Fig. 2. The block diagram of the proposed RF interface.

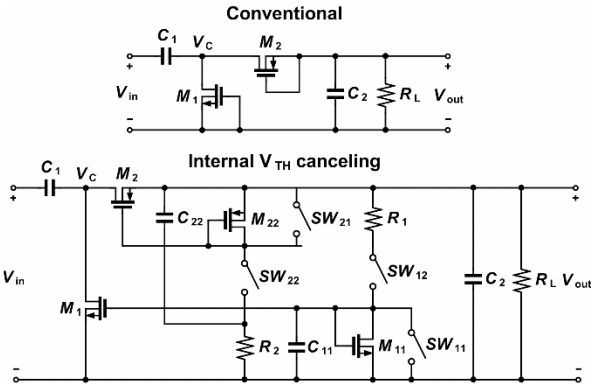

Fig. 3. The schematics of the rectifiers that adopts the conventional and the internal V_{TH} canceling structures.

for type-B [4, 5]. In case of type-A, it is relatively easy to sense signals while the efficiency of supply power generation is low and it is difficult to generate clock to operate digital block [7]. On the other hand, for type-B, it is easy to generate supply power and clock while signal sensing becomes difficult, especially under PVT variation condition [6, 8]. In this paper, we adopts the internal V_{TH} canceling rectifier [9] based on voltage doubler whose power conversion efficiency is high enough to overcome the difficulty of supply generation in ISO 14443 type-A. Additionally, we propose a RF interface structure complementing all drawbacks by proposing the loop-adjustable PLL which allows to generate a stable clock despite 100% ASK signal.

The remainder of this paper is organized as follows. Section II describes the proposed RF interface based on the high efficiency rectifier, the loop-adjustable PLL and their operational principles. Section III shows the experimental results for the implemented RF interface and section IV concludes the paper.

II. Proposed RF Interface Based on High Efficiency Rectifier and Loop-adjustable PLL

Fig. 1 depicts the block diagram of the near field communication (NFC) system for sensors. As shown in the Fig. 1, NFC reader generates an induced current to the RF interface as the way generating the magnetic field from the initial inner coil (LF, HF) or radiating the magnetic field through backscatter (UHF). By rectifying this current the RF interface generates the supply voltages (VDD_A and VDD_D) that are required to operate the circuits in the RF interface, sensor analog front-end (AFE) and the control unit. At this time, the data recognized by the sensor is transformed into the electrical signal (D_IN) through the sensor AFE and then it is transmitted to the RF interface. Fig. 2 depicts the block diagram of the proposed RF interface. As shown in the Fig. 2, the RF interface consists of a clock generator, a rectifier, a RF limiter, a load modulator, low-dropout regulators (LDO), and a demodulator. From RF_IN, the rectifier generates supply voltages for LDO, demodulator, and CLK generator. LDO generates 1.8 V and 2.5 V for the analog and digital supplies of the sensor AFE and the control unit respectively. The demodulator demodulates and transmits the received data to the sensor AFE. The proposed NFC RF interface adopts a high efficiency rectifier based on the voltage doubler to generate the stable supply in a weak field. Besides, for the stable clock generation against inconsistent input data (D_IN) and thus to satisfy ISO14443 type-A, the phase locked loop (PLL) is designed to be loop-adjustable, which allows the PLL loop only turns on when the input data is

'1'. Fig. 3 depicts the schematics of the rectifiers that adopt the conventional and the internal V_{TH} canceling structures respectively. For the rectifier that adopts the conventional voltage doubler, the magnitude of output voltage is limited by 2 V_{in} - (V_{TH_N} - V_{TH_P}) because it uses two diode-connected transistors where V_{TH_N} and V_{TH_P} are the threshold voltages of n- and p-MOSFET, respectively. Therefore, the conventional structure makes it difficult to generate the required supply in a weak field. On the other hand, for the internal V_{TH} canceling (IVC) structure, it minimizes the the output voltage loss caused by the threshold voltage and furthermore lowers the effective threshold voltage of transistors by using four switches (SW_{11}, SW_{12}, SW_{21} and SW_{22}) based on IVC system [9, 10]. This enhances the power conversion efficiency by minimizing reverse leakage current with applying a voltage pulse instead of constant voltage to the transistor gate unlike the previous IVC technique [10]. As shown in the Fig. 3, there are two IVC cells and hence a total of four switches (SW_{11}, SW_{12}, SW_{21} and SW_{22}) are needed. In the first cell, since SW_{11} is 'off' and SW_{12} is 'on' while M_1 is 'on', it shows general IVC operation as the constant voltage is applied to the M_1 gate. Meanwhile, when SW_{11} turns 'on' and SW_{12} turns 'off' while M_1 is 'off', the IVC cell is disconnected with M_1 gate and M_1 gate is grounded through SW_{11}. In this process, the gate voltage of M_1 is applied as the form of pulse, V_{G1}, where its amplitude is 0~ V_{TH_N}. For M_2, the pulse form of V_{G2} is applied in the same way.

Fig. 4 depicts the simulated output voltage waveforms of the conventional and the internal V_{TH} canceling structures. As shown in the Fig. 4, in the conventional structure, the constant voltage is applied to the transistor gate and it generates 0.55 V output voltage based on 1 V peak-to-peak sine wave input. Meanwhile, for the proposed IVC structure, the pulse form of voltage is applied to the transistor gate and hence it generates 0.9 V output voltage under the same conditions, which means the power conversion efficiency (PCE) is improved from 49% to 80%.

Fig. 5 is the block diagram of the proposed low power PLL to generate a stable clock from the 100% ASK input signal as a reference clock. Since the reference frequency (f_{REF}) and VCO frequency (f_{VCO}) are same, the PLL is designed in a integer type. Basically, since 100% ASK signal shows no signal when the data is '0', it is obvious

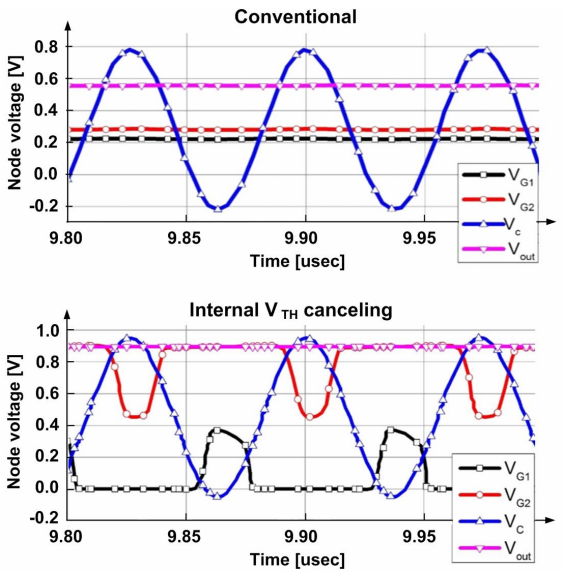

Fig. 4. The simulated output voltage waveforms of the conventional and the internal V_{TH} canceling structures.

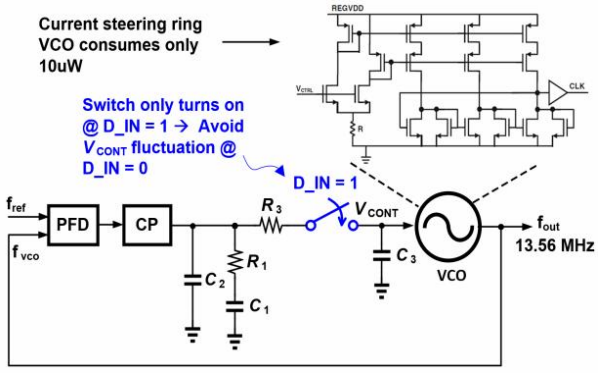

Fig. 5. The block diagram of the proposed low power PLL.

that PLL can not be locked steadily. In order to solve this issue, we propose the switched loop PLL. The PLL loop is only closed when the received ASK signal is '1'. Otherwise, the loop is switched off and keeps the electric charge that has already been charged on the capacitor (C_3) at the edge of the loop filter, thus allowing the VCO to generate the locked frequency. Additionally, the proposed PLL employs a current steering type of ring VCO [11] for a low power implementation as seen in Fig. 5 and it only consumes less than 10 uW.

Fig. 6 depicts the block diagram of the demodulator and the schematic of the envelope detector. The envelope detector is simply designed with a total of four transistors where M_1 plays the role of a rectifier using diode-connection, and M_2 acts as a capacitor. M_3 and M_4 minimize the leakage current by using diode-connected

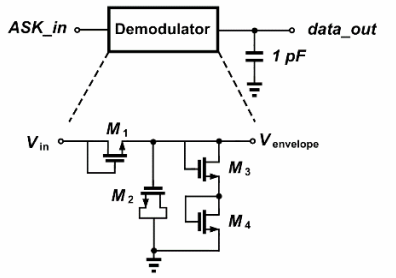

Fig. 6. The block diagram of the demodulator and the schematic of the envelope detector.

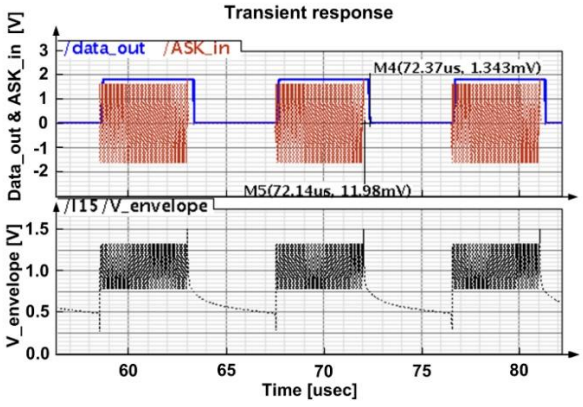

Fig. 7. The simulated output waveform of the demodulator.

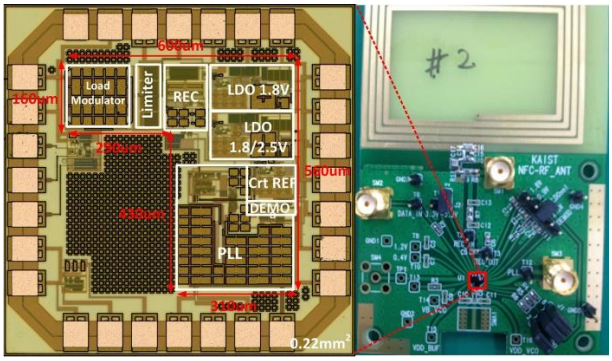

Fig. 8. The micrograph of the proposed RF interface chip and the photo of the implemented NFC tag with an external coil.

transistors instead of resistors. The simulation results with 1 pF capacitor in the load are shown in Fig. 7, which verify that the output of envelope detector (V_envelope) and demodulated output (data_out) come out properly on the 100% ASK input signal (ASK_in).

III. Experimental Results

Fig. 8 shows the micrograph of the proposed RF interface chip and the photo of the implemented NFC tag

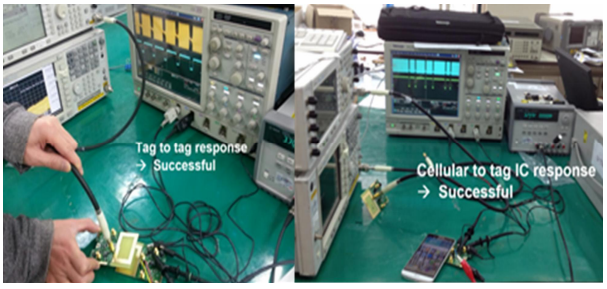

Fig. 9. The demonstration of tag-to-tag and cellular phone-to-tag responses.

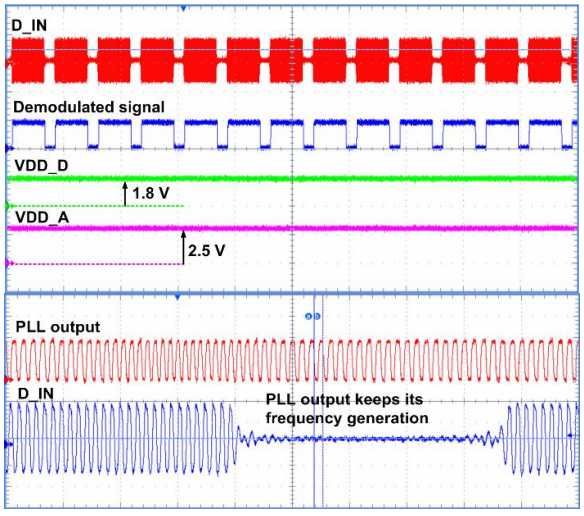

Fig. 10. The measured demodulated signal, generated power, and clock signal.

with an external coil. The chip, implemented in a 0.18 um CMOS process, has been basically tested in tag-to-tag response and additionally confirmed in tag-to-cellular response as shown in Fig. 9. We can verify that the signal is modulated and demodulated while PLL and LDO (2.5 V) work properly in the input signal over 6 dBm. The demodulator and LDO (1.8 V) operation has been confirmed in the input signal over 8 dBm. Fig. 10 shows the measured demodulated signal, generated power, and clock signal where demodulation of the signal in 8 dBm of input power. As shown in Fig. 10, for D_IN is '0', PLL output provides a normal waveform and we can verify that demodulation is done in 100% ASK signal. Fig. 11 shows the measured load modulation and its spectrum. As shown in the Fig. 11, the measurement result shows the modulation depth is about 3.7% that is -28 dBc in the measured frequency spectrum.

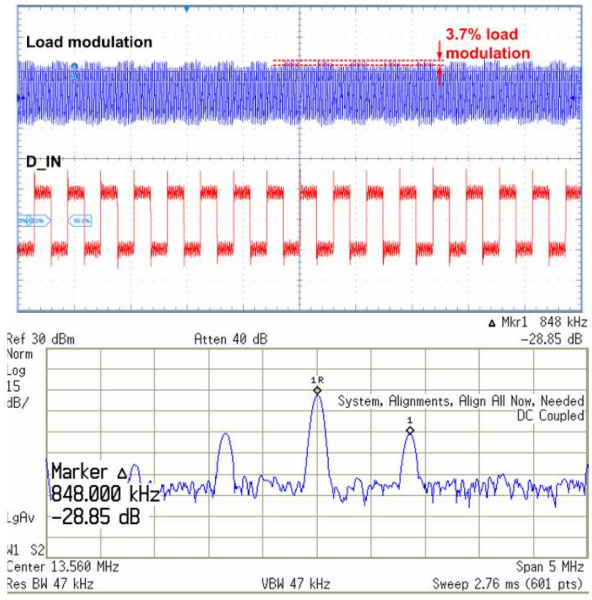

Fig. 11. The measured load modulation and its spectrum.

IV. CONCLUSIONS

In this paper, we propose the RF interface of NFC tag IC which is necessary for transmitting the results obtained using blood glucose sensor, water quality sensor, gas sensor and radioactive sensor to portable devices such as mobile phones. The proposed RF interface complies with the ISO14443 type-A standard using 100% ASK and solves the power and clock generation difficulties by using the internal V_{TH} canceling rectifier that is based on the high efficiency voltage doubler and the switching phase locked loop. In the measurement results, the internal VTH canceling rectifier in the RF interface shows more than 80% power efficiency from 100% ASK signal, and successfully generates 1.8 V / 2.5 V supply from the input signal power higher than 6 dBm through low loss voltage regulator. Additionally, we can verify that the proposed switching phase locked loop is locked at 8 dBm or higher input signal power and successfully demodulates ASK input signal.

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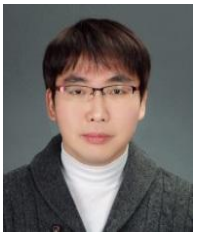

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