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Optimization of Dual-workfunction Line Tunnel Field-effect Transistor with Island Source Junction

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***Abstract*—In this research, a novel dual workfunction (DWF) line tunnel field-effect transistor (LTFET) is optimized by using high WF gate-drain underlap and low WF gate-source underlap. Through numerical technology computer-aided design (TCAD) device simulations, it is confirmed that on-current (I_{ON}) can be increased by highly localized point tunneling while suppressing off-current (I_{OFF}) by adjusting the distance between low-WF gate and source junction. Considering on-off current ratio (I_{ON}/I_{OFF}) and the process variation, the distance between high-WF gate and source junction is optimized to be 3 to 5 nm.**

***Index Terms*—Dual workfunction, line tunneling field-effect transistor (LTFET), junction underlap, TCAD device simulation, low-power operation**

I. INTRODUCTION

Tunneling field-effect transistor (TFET) has been widely studied to overcome the physical limitation in which subthreshold swing (S) of metal-oxide-semiconductor field-effect transistor (MOSFET) is not permitted to be below 60 mV/dec at room temperature [1-3]. However, its rather low on-state current (I_{ON}) driven by band-to-band tunneling (BTBT) has been pointed out as a weak point. In order to enhance the current drivability of TFET, line tunneling field-effect transistor (LTFET) was proposed in the previous literature [4]. Also, it was reported that adopting gate with different workfunctions, dual-workfunction (DWF) gates, improved the current characteristics [5-9]. When DWG is applied to LTFET, the electrical characteristics vary greatly depending on important parameters such as the structure of the source region or the length of two gates, but there has been no detailed analysis on the optimization of this structure. Therefore, in this paper, optimal design of a DWF LTFET has been performed, and as the results, improvements of on-off current ratio (I_{ON}/I_{OFF}) and S have been achieved. The key solution lies in the engineering over the source-drain underlap in the DWF LTFET structure, which has been confirmed by series of numerical technology computer-aided design (TCAD) device simulations.

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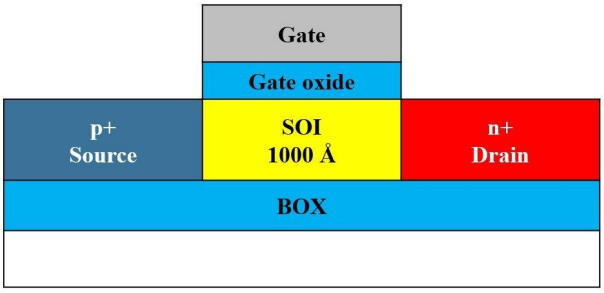
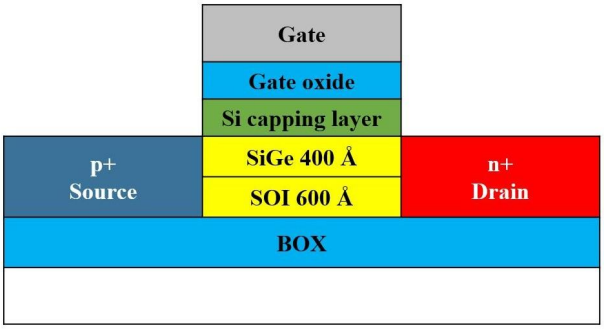
II. TUNNELING MODEL CALIBRATION

In order to calibrate the BTBT model using Sentaurus tools [10], the planar Si and SiGe TFETs are fabricated as shown in Fig. 1(a) and (b). In the case of Si TFET, SOI source implantation and drain implantation with As is used at the same conditions. For comparison, SiGe TFET consists of 40 nm thickness $Si_{0.7}Ge_{0.3}$ layers on SOI (100) substrates which are lightly p-doped (1×10^{15}



(a)



(b)

Fig. 1. Cross-sectional views of the (a) Si TFET; (b) SiGe TFET.

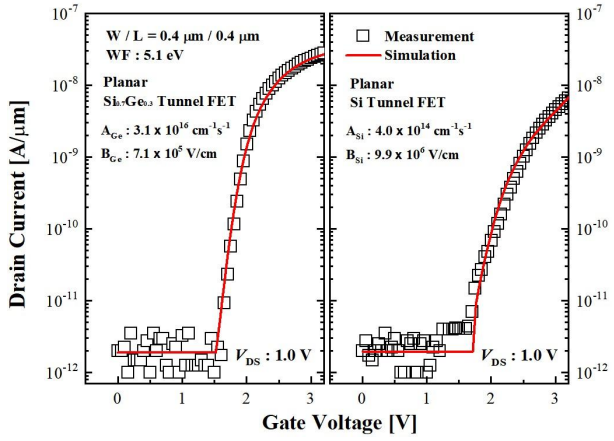


Fig. 2. Calibrated transfer curves of SiGe and Si TFET.

cm^{-3}) with 60 nm thickness and Si capping layer is grown on the SiGe channel and 200 nm thickness poly-Si gate and 3 nm SiO_2. The transfer characteristic of the fabricated Si and SiGe TFETs which have both 400 nm gate length and width are measured at the drain voltage (V_{DS}) of 1.0 V.

Kane's BTBT model is calibrated to the measured result of the fabricated Si and SiGe TFETs. The BTBT generation rates (G) per unit volume in this model are defined as

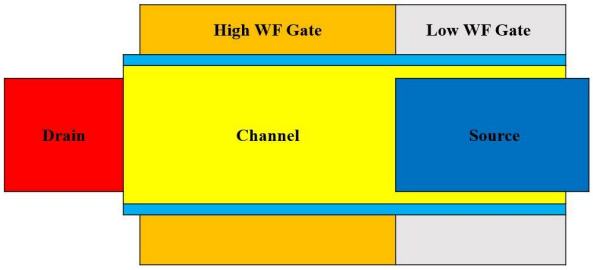


Fig. 3. Basic structure of the device.

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right)$$

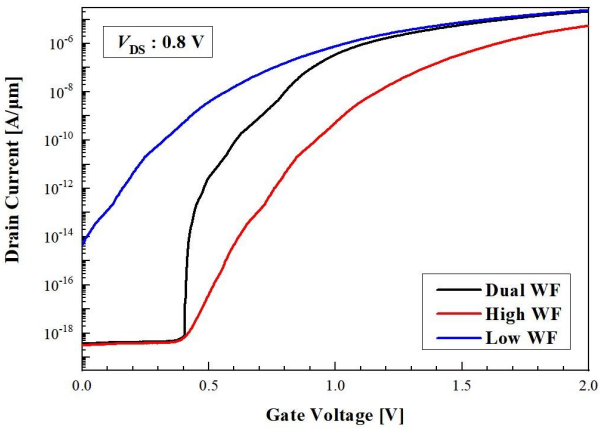
in the uniform electric field limit where F_0 = 1 V/m and P = 2.5 for indirect BTBT [10]. A of the pre-factor and B of the exponential factor are the Kane parameters while F is the electric field [11, 12]. As mentioned above, several simulations are performed to fit the measured data by adjusting the A and B parameters. The A and B values are chosen as for optimal fit according to the results between the simulated and measured data Fig. 2. It can be seen that the log scale of transfer characteristics is well fitted from the results. The extracted A and B parameters of the BTBT model in Si TFET are 4×10^{14} $cm^{-1}\cdot s^{-1}$ and 9.9×10^6 V/cm, respectively. As SiGe TFET's transfer characteristics, the A and B parameters of Ge can be extracted as 3.1×10^{16} $cm^{-1}\cdot s^{-1}$ and 7.1×10^5 V/cm, respectively.

III. Basic Device Structure

Fig. 3 shows the basic device structure. The extruded source structure reduces the energy band bending of the pn junction where point tunnelling occurs, reducing the hump behavior. And the high WF gate-drain underlap reduces ambipolar current (I_{AMB}) [4]. As drain is far from gate, the electric field applied to drain junction becomes weak. In this research, high WF is set to 5.10 eV and low WF is 4.06 eV, respectively.

IV. Simulation and Results

To confirm the improved S and I_{ON}/I_{OFF}, numerical simulations are conducted by Sentaurus tools. Fig. 4(a) shows the drain current-gate voltage (I_D-V_G)



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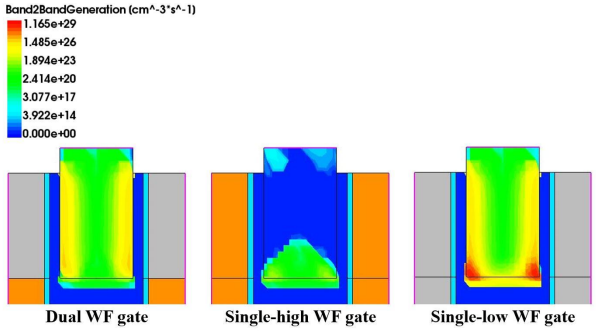
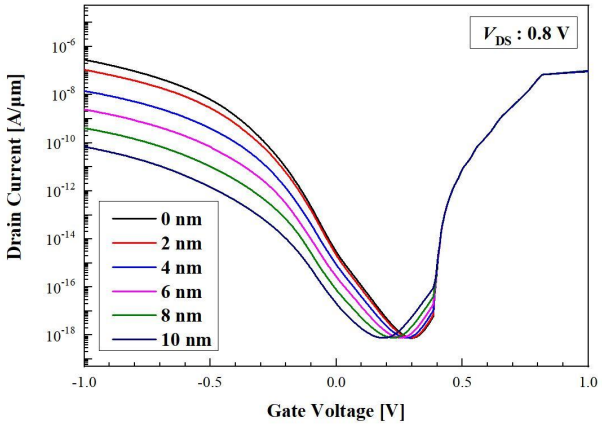


(b)

Fig. 4. (a) Electrical characteristic of dual WF and different WF structures; (b) BTBT generation rate of dual WF and different WF structures at V_{GS} = 0.7 V.

characteristics of different WF and dual WF structures. Fig. 4(b) shows the BTBT generation rate at 0.7 V in this case. Single-high WF gate weakens the electric field applied to source, so less BTBT generation occurs and the total I_{ON} is decreased. And although point tunneling is reduced, line tunneling is also reduced, so it is difficult to expect better S. Single-low WF gate increases the electric field applied to source junction, so a lot of BTBT generation occurs and the total I_{ON} is increased. However, because of the low WF, point tunneling occurs even at 0 V, which increases the off-current (I_{OFF}), and S gets worse. In case of dual gate with low WF and high WF, point tunneling at off-state is suppressed due to high WF gate and line tunneling at on-state is activated due to low WF gate, which improves S. The dual work function structure shows good electrical characteristics, but if point tunneling can be used in I_{ON} while suppressing I_{OFF}, these characteristics can be improved further.

Fig. 5(a) shows the I_D-V_G characteristic according to



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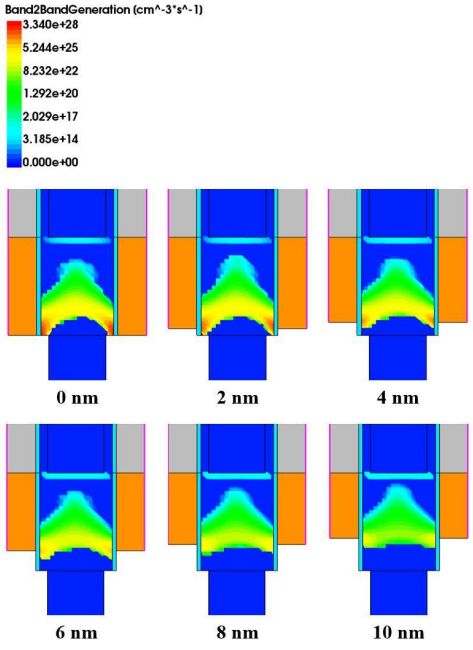


(b)

Fig. 5. (a) Electrical characteristics by changing the distance between high WF gate and drain; (b) BTBT generation rate of high WF gate-drain underlap structures at V_{GS} = -0.5 V.

the distance between high WF gate and drain. Fig. 5(b) shows the BTBT generation rate at -0.5 V in this case. As the drain underlap length increased from 0 nm to 10 nm, the hole tunneling is efficiently decreased and I_{AMB} is also reduced.

Fig. 6(a) shows the I_D-V_G characteristic according to the distance between high WF gate and source. Fig. 6(b) shows the BTBT generation rate at 0.7 V in this case. It is confirmed that I_{OFF} decreased as source underlap length increased from 0 nm to 10 nm. It shows that I_{ON}/I_{OFF} is improved when the high WF gate underlap

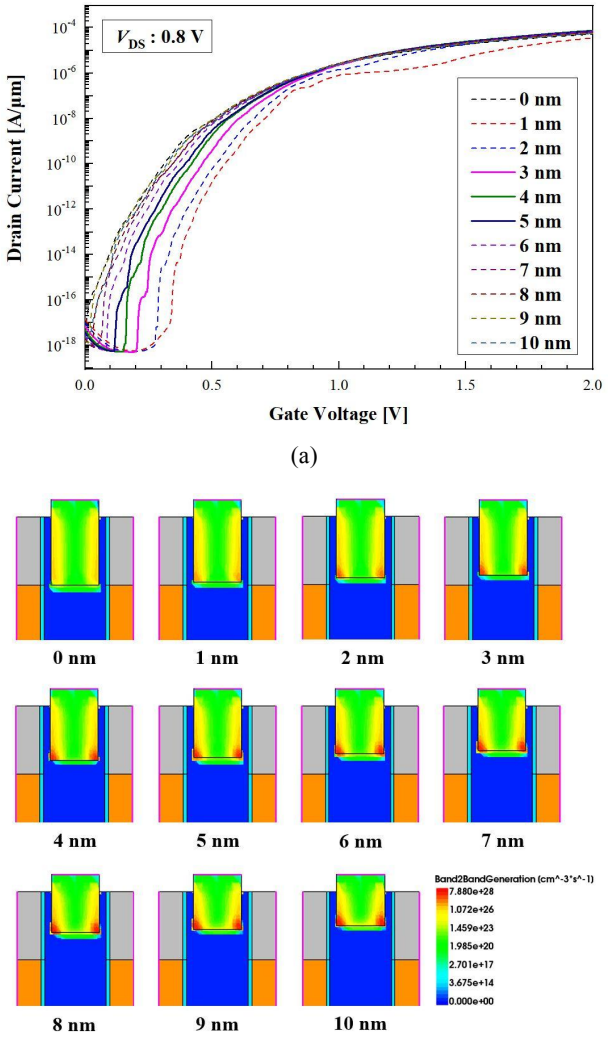


Fig. 6. (a) Electrical characteristics by changing the distance between high WF gate and source; (b) BTBT generation rate of low WF gate-source underlap structures at V_{GS} = 0.7 V.

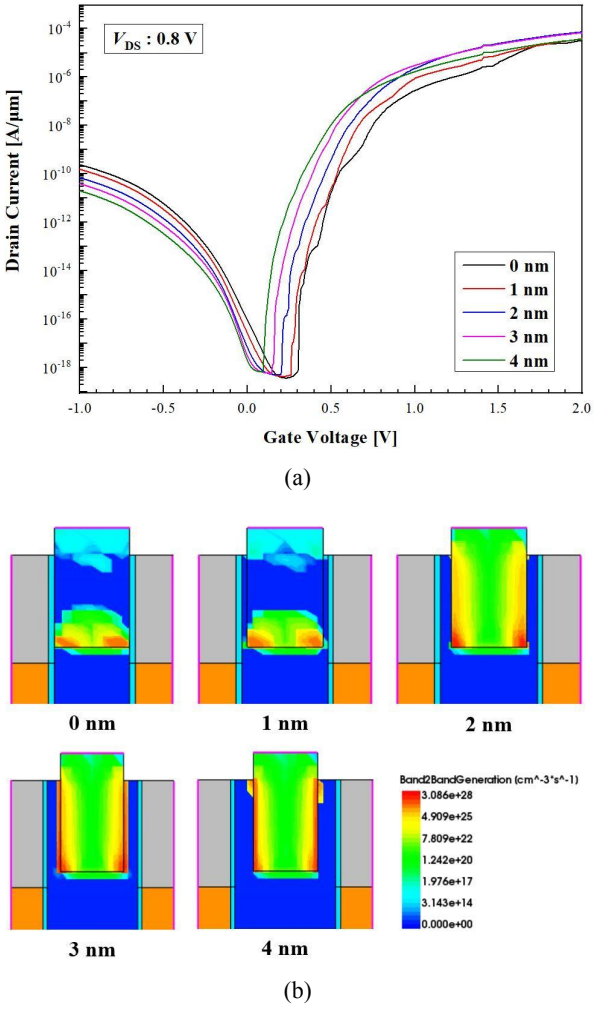
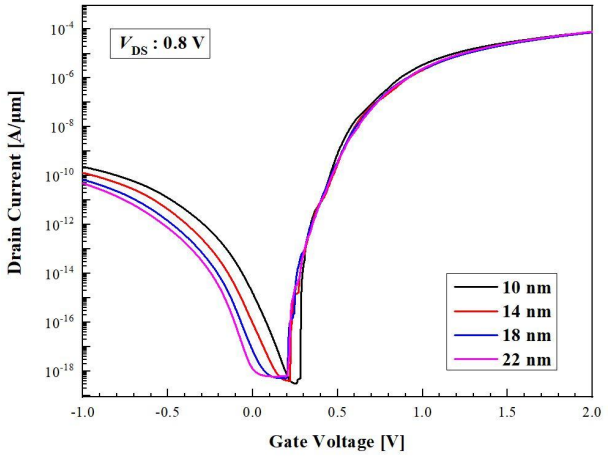


Fig. 7. (a) Electrical characteristics by changing vertical tunneling length; (b) BTBT generation rate at V_{GS} = 0.7 V.

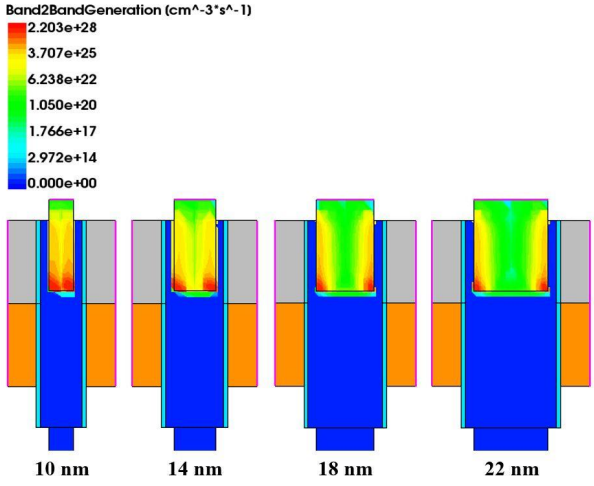
length is 3 nm to 5 nm compared to 0 nm to 2 nm. However, if the high WF gate underlap length is more than 6 nm, there is a possibility that I_{OFF} increases rapidly because of the process variation. Therefore, a gate underlap length between 3 nm to 5 nm is suitable. As a result, it is confirmed that I_{ON} can be increased by using point tunneling while suppressing I_{OFF}.

Fig. 7(a) shows the I_D-V_G characteristic according to vertical tunneling length and Fig. 7(b) shows the BTBT generation rate at 0.7 V in this case. When the vertical tunneling length is 0 nm to 1 nm, line tunneling do not occur at V_{GS} = 0.7 V. This is because there is not enough space for line tunneling to occur. When the vertical tunneling length becomes 2~3 nm, line tunneling occurs as the gate voltage increases, and as a result, high I_{ON} can be obtained. However, when the vertical tunneling length is increased to 4 nm, the drain current at high voltage is rather decreased. This is because the width of the tunneling barrier increases as the depletion region increases.

Fig. 8(a) shows the I_D-V_G characteristic according to body thickness and Fig. 8(b) shows the BTBT generation rate at 0.7 V in this case. It is purpose to minimize the device size without causing performance degradation. First, in the case of I_{ON}, even if the body thickness is reduced from 22 nm to 10 nm, there is no significant difference. On the other hand, it shows that I_{AMB} increases as body thickness decreases from 22 nm to 10 nm. However, this problem can be improved through drain underlap length. Through additional simulations,



(a)



(b)

Fig. 8. (a) Electrical characteristics by changing body thickness; (b) BTBT generation rate at V_{GS} = 0.7 V.

when the drain underlap length is 10 nm, it is confirmed that there is no increase in I_{AMB} even when the body thickness is reduced to 14 nm. As a result, the total body thickness is reduced from 20 nm to 14 nm.

V. Viable Process Integration

Fig. 9(a)-(d) show the process of LTFET fabrication. Fig. 9(a) shows that the drain, body and source regions are sequentially grown through the epitaxy process [13, 14]. Fig. 9(b) shows active patterning and device isolation process [15]. Fig. 9(c) shows that the vertical tunneling region is formed through Si-epitaxy. Finally, the proposed device fabrication is completed with gate oxide growth and gate patterning process as shown in Fig. 9(d).

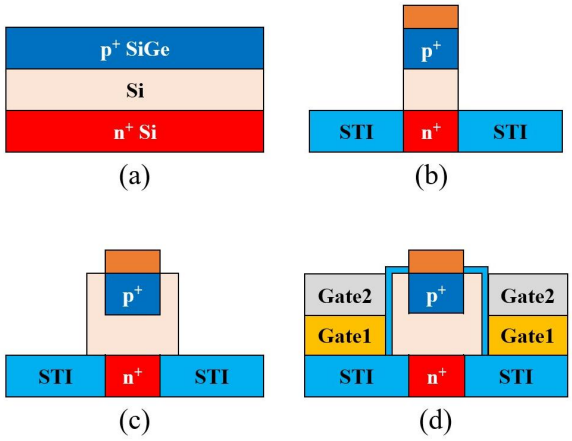


Fig. 9. Fabrication process flow of the proposed device.

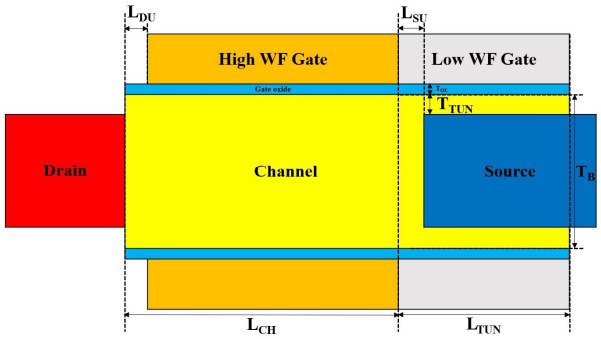


Fig. 10. Optimized structure of the device.

Table 1. Parameters of the optimized device used for numerical simulation

Parameters	Definitions	Value
N_S	Source doping concentration (Boron)	10^{20} cm^{-3}
N_{CH}	Channel doping concentration (Arsenic)	10^{17} cm^{-3}
N_D	Drain doping concentration (Arsenic)	10^{20} cm^{-3}
L_{SU}	Source underlap length	3 nm
L_{DU}	Drain underlap length	10 nm
T_B	Body thickness	14 nm
T_{OX}	Gate oxide thickness	1 nm
L_{CH}	Channel length	30 nm
L_{TUN}	Vertical tunneling length	20 nm
T_{TUN}	Vertical tunneling thickness	2 nm
V_{DS}	Drain voltage	0.8 V
WF_1	High work function (Gate 1)	5.10 eV
WF_2	Low work function (Gate 2)	4.06 eV

VI. Conclusions

Table 1 shows the optimized device parameters used for numerical simulation. Fig. 11 shows the I_D-V_G characteristic of control device and optimized device (Fig.

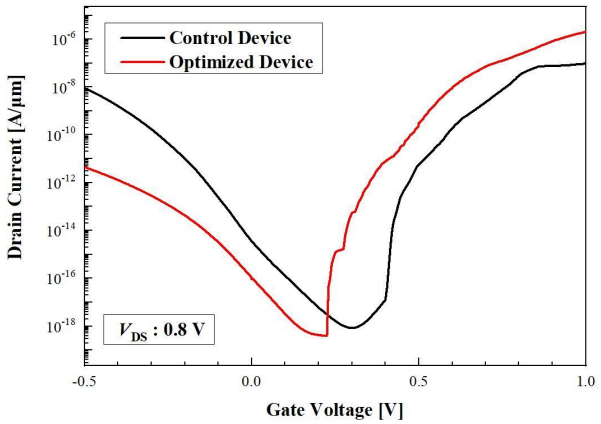


Fig. 11. Electrical characteristic of control device and optimized device.

10). A source and drain underlap on DWF LTFET is optimized. And a control device is the structure without high WF gate-drain underlap and low WF gate-source underlap in Fig. 3. By numerical simulations, it was confirmed that the source and drain underlap structure can improve the electrical performance at low voltage [16-21]. In particular, the distance between high WF gate and source is suitable to be 3 to 5 nm considering better I_{ON}/I_{OFF} and the process variation.

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REFERENCES

[1] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer: I-MOS: A Novel Semiconductor Device with a Subthreshold Slope Lower than kT/q, IEEE International Electron Device Meeting (IEDM), San Francisco, USA, p. 289, 2002.

[2] S. Cho, I. M. Kang, T. I. Kamins, B.-G. Park, and J. S. Harris: Silicon-compatible compound semiconductor tunneling field-effect transistor for high performance and low standby power operation, Appl. Phys. Lett., vol. 99, p. 243505, 2011.

[3] T. Sakurai: Perspectives of low-power VLSI's. IEICE Trans. Electron., vol. E87C(4), p.429, 2004.

[4] A. M. Walke, et al.: Fabrication and Analysis of a Si/Si0.55Ge0.45 Heterojunction Line Tunnel FET, IEEE Trans. Electron Devices, vol. 61, p. 707, 2014.

[5] Y. S. Kwon, S. -H. Lee, Y. Kim, G. Kim, J. H. Kim, S. Kim: Surrounding Channel Nanowire Tunnel Field-Effect Transistor with Dual Gate to Reduce a Hump Phenomenon, J. Nanosci. Nanotechnol., vol. 20, p. 4182, 2020.

[6] Kim, H.W., Sun, M.C., Kim, S.W. and Park, B.G.: Hump Phenomenon in Transfer Characteristics of Double-Gated Thin-Body Tunneling Field-Effect Transistor (TFET) with Gate/Source Overlap, IEEE 5th International Nanoelectronics Conference (INEC), Singapore, Singapore, pp. 364-366, 2013.

[7] Lee, J.C. and Yu, Y.S.: Work-function engineering of source-overlapped dual-gate tunnel field-effect transistor, Journal of Nanoscience and Nanotechnology (JNN), vol. 44, pp. 90-101, 2018.

[8] Prabhat Singh, Dharmendra Singh Yadav.: Impact of work function variation for enhanced electrostatic control with suppressed ambipolar behavior for dual gate L-TFET, Current Applied Physics, vol. 44, pp. 90-101, 2022.

[9] Yun, C., Cho, S., Cho, I. H. and Kim, G.: Hump Phenomenon in Transfer Characteristics of Double-Gated Thin-Body Tunneling Field-Effect Transistor (TFET) with Gate/Source Overlap, 2022 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD), July 7-8, Busan, Korea, 2022, pp. 1-2.

[10] Sentaurus Device, Synopsys, Version P-2019.03, Synopsys Inc.

[11] Kane, E., Theory of tunneling: Journal of Applied Physics, 32(1), pp. 83-91, 1961.

[12] Biswas, A., Dan, S., Royer, C., Grabinski, W. and Ionescu, A.: TCAD simulation of SOI TFETs and calibration of non-local banc-to-band tunneling model, Microelectronic Enginnering, 98, pp. 334-337, 2012.

[13] Shogo Fukami, Yoshihiko Nakagawa, Mel F. Hainey Jr., Kazuhiro Gotoh, Yasuyoshi Kurokawa, Masahiro Nakahara, Marwan Dhamrin and Noritaka Usam.: Epitaxial growth of SiGe on Si substrate by printing and firing of Al-Ge mixed

paste, Japanese Journal of Applied Physics, vol. 58, no. 4, 2019.
[14] Takahiro Tsukamoto, Yosuke Aoyagi, Shouta Nozaki, Nobumitsu Hirose, Akifumi Kasamatsu, Toshiaki Matsui, Yoshiyuki Suda.: Increasing the critical thickness of SiGe layers on Si substrates using sputter epitaxy method, Journal of Crystal Growth, vol. 600, 2022.
[15] X. Liu, K. Lim, Z. Wu, Z. Xiong, Y. Ding, H. Nong.: A Study of Inverse Narrow Width Effect of 65nm Low Power CMOS Technology, Incorporating Knowledge in Genetic Algorithms for Device Synthesis, pp. 1138-1141, 2008.
[16] Cheung, K.T: On the 60 mV/dec@300 k Limit for MOSFET Subthreshold Swing, Symposium on VLSI Technology (VLSIT), Ap, Hsinchu, Taiwan, pp. 72-73, 2010.
[17] Huang, Q., Huang, R., Zhan, Z., Qiu, Y., Jiang, W., Wu, C. and Wang, Y.: A Novel Si Tunnel FET with 36 mV/dec Subthreshold Slope Based on Junction Depleted-Modulation Through Striped Gate Configuration, IEEE International Electron Device Meeting (IEDM), San Francisco, CA, USA, pp. 187-190, 2012.
[18] Choi, W.Y., Park, B.G., Lee, J.D. and Liu, T.J.K.: Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec, IEEE Electron Device Letters, 28(8), pp. 743-745, 2007.
[19] Iman Chahardah Cherik, Saeed Mohammadi, Ali Asghar Orouji.: Switching Performance Enhancement in Nanotube Double-Gate Tunneling Field-Effect Transistor With Germanium Source Regions, IEEE Transactions on Electron Devices, vol. 69, pp. 364-369, 2021.
[20] Faraz Najam, Sangwan Kim, Woo Young Choi, Yun Seop Yu.: Physically Consistent Method for Calculating Trap-Assisted-Tunneling Current Applied to Line Tunneling Field-Effect Transistor, IEEE Transactions on Electron Devices, vol. 67, pp. 2106-2112, 2020.
[21] Chander, S., Sinha, S.K., Chaudhary, R.: Ge-Source Based L-Shaped Tunnel Field Effect Transistor for Low Power Switching Application, Silicon 14, pp. 7435-7448, 2022.

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