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A 16 GHz 1-511 Broadband Programmable Frequency Divider

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***Abstract*—A high-speed broadband programmable frequency divider chip is designed and implemented in 0.18 μm SiGe BiCMOS process. The chip is based on the 2/3 dual-mode frequency divider, and integrates high-speed logic operation and reset control in the flip-flop to achieve a wide range of continuous integer frequency division ratio. Taking SCFL and CML DFF as basic units, it realizes wide-band operation and obtains a good input sensitivity range. The test results demonstrate that the operating frequency covers 0.1 GHz to 16 GHz. The frequency divider achieves 1-511 continuous frequency division. The output signal phase noise of the 1 GHz input is -153.7 dBc/Hz @ 100 kHz offset in divide-by-8 mode.**

***Index Terms*—Integrated circuit, frequency divider, broadband, programmable, SiGe**

I. INTRODUCTION

With the gradual increase in the operating frequency of the communication systems, the requirements for the operating frequency of the phase-locked loop (PLL) circuit are also gradually increased. The frequency divider is an important part of the PLL circuit, by which the overall performance of the PLL is directly determined. In general, the frequency divider is required to cover the widest possible frequency band, the largest possible frequency divider ratio, and the excellent input sensitivity so as to maximize its application range. Therefore, investigation on the high frequency broadband programmable frequency divider is a hotspot in this field [1-5].

Based on the scalable multi-mode frequency divider structure, this paper designs a high-frequency broadband programmable frequency divider of 1-511 division ratio, with the duty cycle being close to 50%. In modern communication systems and instruments, frequency dividers with a wide range of continuously programmable frequency divisions are required in both local oscillator sources and PLL sources. In this sense, the present work is suitable for applications in these fields.

II. ARCHITECTURE DESIGN

The programmable frequency divider with a wide division ratio range usually adopts a 2/3 frequency divider cascade structure. This structure has the advantages of high reusability and easy expansion, but it needs to be optimized so as for the requirements of any frequency division ratio.

1. Traditional 2/3 Divider Cascade Structure

The realization of programmable continuous frequency division based on the 2/3 divider cascade structure [6, 7], is shown in Fig. 1.

The principle of the basic unit circuit 2/3 frequency

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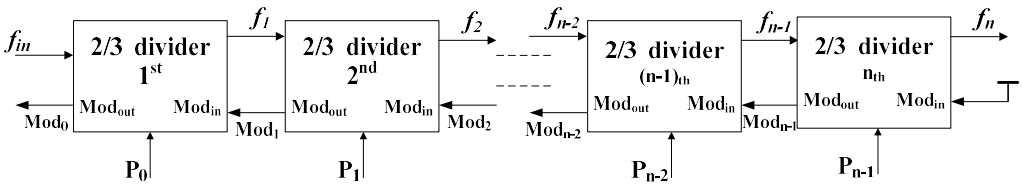


Fig. 1. Programmable frequency divider circuit based on 2/3 frequency divider stage.

divider is that when Mod_{in} is low, the circuit realizes 2 division; when Mod_{in} is high, the frequency division ratio realized is related to the control P_i: when P_i=0, it realizes 2 division; when P_i=1, it realizes 3 division. Therefore, the actual output frequency f_i of the ith 2/3 divider unit circuit is:

$$f_i = \frac{f_{i-1}}{2 + P_{i-1} \cdot Mod_{in}} \tag{1}$$

where f_{i-1} is the input frequency and $f_0 = f_{in}$.

The total frequency division ratio of multi-mode frequency divider cascaded by n-stage 2/3 frequency divider units is:

$$M = P_0 + 2 \cdot P_1 + 2^2 \cdot P_2 + \cdots + 2^{n-2} \cdot P_{n-2} + 2^{n-1} \cdot P_{n-1} + 2^n \tag{2}$$

It can be deduced from Eq. (2) that the maximum and minimum frequency division ratios achieved by this structure are 2^{n+1}-1 and 2^n, respectively. In addition, the ratio of the maximum frequency division to the minimum frequency division is approximately 2. Consequently, the frequency division ratio range is limited. Therefore, in order to achieve the frequency division ratio below 2^n, the above architecture needs to be optimized.

2. Multi-mode Frequency Divider with Expandable Frequency Division Ratio

On the basis of the circuit structure of Fig. 1, this article incorporates the corresponding logic operation to realize a multi-mode frequency divider with an arbitrarily expandable frequency division ratio, thereby achieving a continuous programmable frequency division ratio range from 1 to 511 ultimately. The specific structure is shown in Fig. 2. Compared with the traditional structure shown in Fig. 1, the proposed structure can achieve a significantly wider frequency division ratio. It can start with a continuous integer frequency division ratio starting from 1, and the maximum frequency division ratio can be expanded arbitrarily with the extension of the circuit, thereby showing better flexibility and versatility.

The structure consists of the selective trigger module, the frequency division link, and the input logic module, as shown in the upper, middle, and bottom parts of Fig. 2, respectively. The selective trigger module makes the duty cycle of the output waveform close to 50% through proper logic operation and trigger control. In contrast, the traditional topology would lead to the obvious duty cycle imbalance of the output waveform. The frequency division link is the core part of the whole circuit, completing the operations of high-speed frequency division and pulse swallowing.

By designing appropriate logic operations, the frequency division link can break through the lower limit of conventional frequency division ratio and completely cover 1 to 511.

The proposed structure adds a control terminal P_n and an additional combinational logic circuit on the traditional 2/3 frequency divider cascade structure to expand the frequency division ratio. Assuming that the mod input of the n'th 2/3 frequency divider unit is set as valid, and all the units on the right side are made invalid through the combinational logic and control terminal, the effective number of cascaded 2/3 frequency dividing units is n'. Therefore, the lowest frequency division ratio of the programmable frequency divider is $2^{n'}$. Herein, n' is called the effective length of the programmable frequency divider. If the above-mentioned control logic makes all the mod signals valid, the highest divider ratio becomes 2^{n+1}-1. It can be found that the maximum and minimum frequency division ratios are related to n and n', respectively. The frequency division ratio of the above

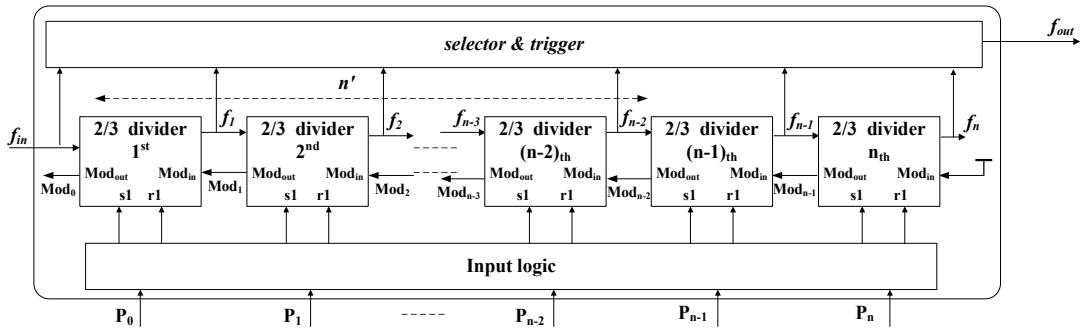


Fig. 2. Multi-mode frequency divider circuit with expandable frequency division ratio.

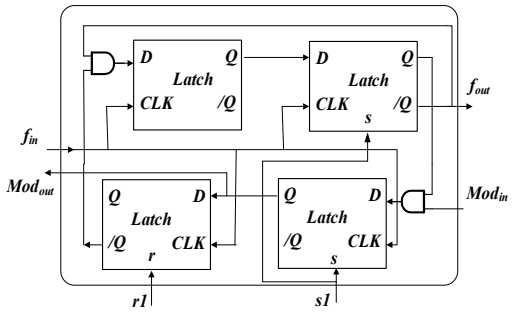


Fig. 3. Block diagram of the 2/3 divider.

circuit can be expanded easily by choosing the values of n and n' appropriately. The state of each 2/3 frequency dividing unit can be controlled by the two reset signals *r1* and *s1*, which are obtained from the combinational logic of the external mode control terminals P_0~P_n.

The above circuit optimization is easy to be implemented by adding simple combinational logic only. Meanwhile, the advantages of the traditional 2/3 frequency divider such as simple structure, low parasitic, and reusability are retained.

Furthermore, the above circuit also includes a module that can adjust the traditional imbalanced duty cycle of output signal to be approximately 50% through inner clock triggering and reshaping, as described in the section below.

III. CIRCUIT DESIGN

It can be seen from Fig. 2 that the crucial parts of the structure are the 2/3 dual-mode frequency divider unit and the implementation of pulse swallow [7-9]. Fig. 3 shows the block diagram of the optimized 2/3 dual-mode frequency divider unit. It includes D flip-flops and two logic gates. The built-in reset signal can control the 2/3 divider cell to work in the reset state and the normal state. Compared with the traditional three logic gates [7-9], this reset control can not only save a logic gate but more importantly, can effectively reduce the loop delay time. This is very effective for increasing the maximum operating frequency of the divider unit. Through a combinational logic cell, the external control signal P_n decodes the appropriate reset signals *r1* and *s1*. These reset signals and the mode signal Mod_{in} from the pre-stage determine whether the current stage circuit implements division by 2 or division by 3.

When the programmable frequency divider is working, if the bits from P_i to P_n are all 0, then each frequency division unit corresponding to P_i to P_n does not work. Therefore, the *s1_i* signal corresponding to the P_i control bit is high, the main frequency division branch of this stage is set to logic high, and the corresponding 2/3 frequency division unit has no output. At the same time, the *s1_i* signal sets the corresponding latch output of Mod_{out} to logic high. Therefore, the *s1_i* signal is the temperature code. If the P_i control bit is low, the corresponding pulse swallow latch is reset to logic low. Therefore, the implementation of the input logic in Fig. 2 can be simplified and is shown in Fig. 4.

In order to achieve the highest possible operating frequency, the D flip-flops of the first-stage 2/3 divider unit utilize the ECL structure. At the same time, in order to minimize the delay of the feedback loop of the prescaler in Fig. 3, the combinational logic is merged into the D flip-flop [10, 11], as shown in Fig. 5. The proposed structure incorporates the necessary logical operations for dual mode prescaler and thus has lower power consumption.

The structure in Fig. 5 can realize the AND operation of input A and input B, which is implemented in the read-

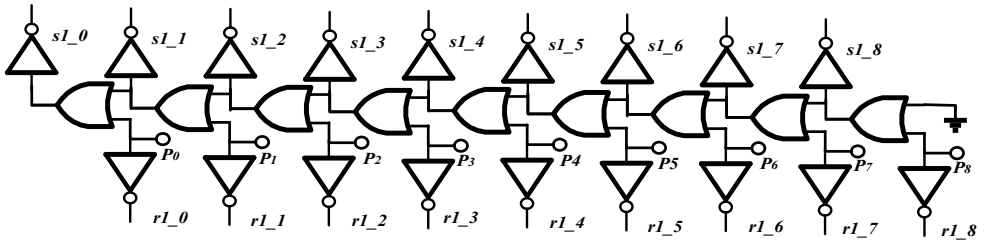
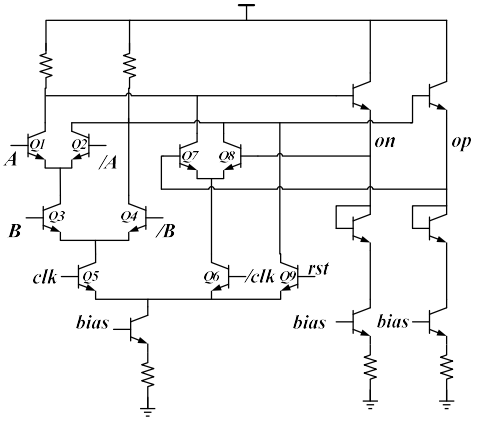


Fig. 4. Input control logic.

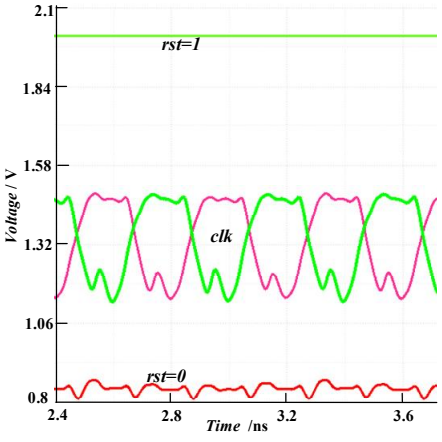
in cycle of the flip-flop. This can eliminate the individual AND gate delay time and effectively improve the maximum operating speed of the frequency divider. Similarly, the overall delay time of the logic controller can also be effectively shortened to achieve the best timing matching with the prescaler module. This can ensure the correctness of the high-frequency swallowing pulse. The reset branch can also be merged into the flip-flop without increasing circuit delay. In contrast, if the reset operation is realized by using a conventional method similar to the *A*/*B* control signal, an additional layer of devices is required, which is very unfavorable for low-voltage applications. Therefore, only parallel devices are used to achieve the reset. Because the transistors of the *clk* signal and the *rst* signal are in the same layer in topology, it is necessary to specially control the high and low level values of the *rst* signal, which are wider than those of the *clk* signal, so as to ensure that tail current can flow correctly between *Q5*/*Q6* and *Q9* devices. If the difference between the voltage of the *rst* signal and the *clk* signal is small, the current would not switch thoroughly, which will affect the correct output voltage.

For the most crucial D flip-flop in the first-stage 2/3 frequency divider, its operating point should be optimized to assure its operating speed greater than 16 GHz. The *Q5*/*Q6* in Fig. 5 are the most important clock switching devices. It is required to adjust them to the proper operating point with high cutoff frequency to meet the speed requirement. At the same time, the load resistance should not be too large, and the signal swing of 100 mV~150 mV is sufficient, which can reduce the circuit delay and power consumption.

When the previous two-stage 2/3 frequency divider works reliably, the operating frequency of the latter 2/3 frequency divider has been reduced to less than 5 GHz. Therefore, the subsequent D flip-flops can use the CML



(a)



(b)

Fig. 5. Flip-flop merged logic gate: (a) Schematic; (b) Signal level.

structure to reduce power consumption. Even, the frequency divider in the last three stages can be realized by using a CMOS circuit structure to further reduce power consumption. In order to maintain the low phase noise characteristics of frequency divider circuits, all frequency dividers in the frequency divider link adopt differential topology and are implemented by triode devices. The first 2/3 frequency divider unit has a power consumption of 17 mW, and the final stage has a power

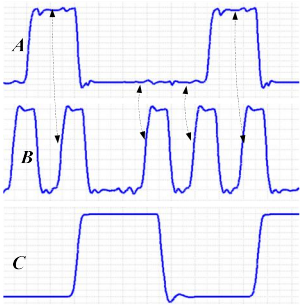


Fig. 6. Output duty cycle adjustment.

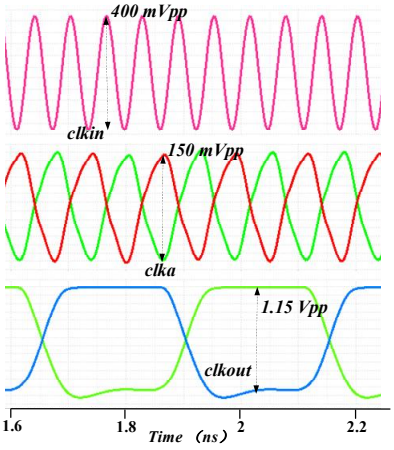


Fig. 7. Simulation results for 16 GHz input.

consumption of 2.6 mW.

Finally, using the pre-divided output clock as a trigger clock can effectively improve the duty cycle of the inner divided signal. The principle is shown in Fig. 6. Herein, *A* is the output frequency division signal of the 2/3 frequency division unit, *B* is the input clock signal of the same 2/3 frequency division unit, and *C* is the output signal that uses the rising edge of *B* to re-trigger the frequency division signal. It can be seen from the figure that the duty cycle adjustment can be well realized by using the duty cycle change of the clock link itself.

Fig. 7 shows the simulation results of the frequency divider in divide-by-8 mode working at a clock frequency of 16 GHz. The top, middle, and bottom subfigures are the input clock *clkin* with an amplitude of 400 mVpp; the first stage 2/3 divider output signal *clka* with an amplitude of 150 mVpp, and the final divide-by-8 output signal *clkout* with an amplitude of 1.15 Vpp, respectively. It is seen from the figure that the first stage 2/3 division signal, which is the most critical, has a swing of around 150 mVpp, indicating that a faster response time and a reliable transmission of high-frequency logic signals can be achieved.

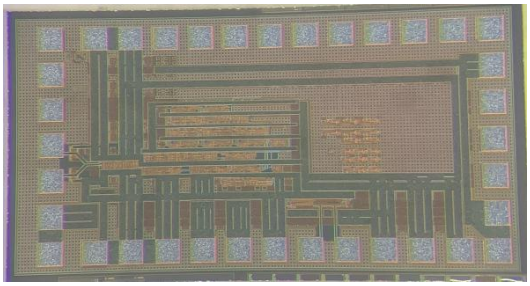


Fig. 8. Photograph of programmable frequency chip.

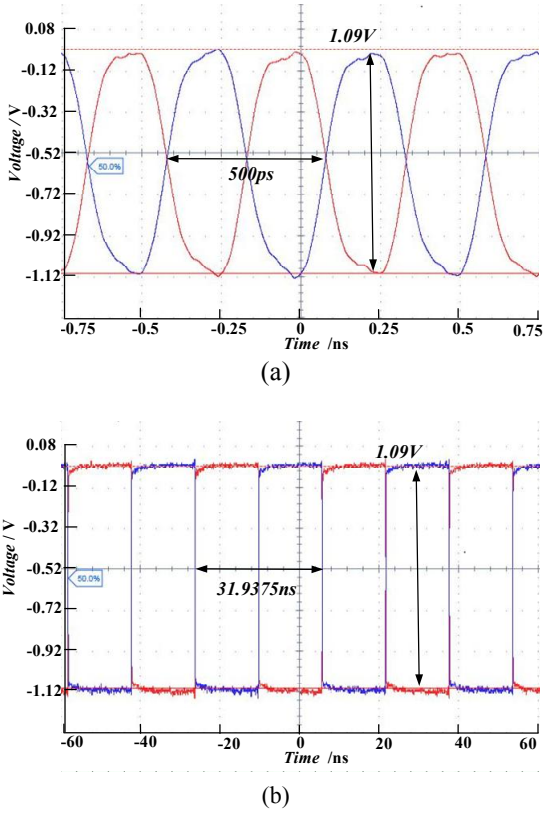


Fig. 9. Test results of 16 GHz input: (a) Divide-by-8; (b) Divide-by-511.

IV. Measurement Results

The chip is implemented in 0.18 μm SiGe BiCMOS process, the frequency divider link is implemented by SiGe HBT device, and the logic control part is implemented by CMOS device. The core area of the chip is 450 μm×350 μm. The entire chip photo is shown in Fig. 8.

The divider is measured with 0 V/-3.3 V power for the testing convenience. Fig. 9 shows the output waveform

Table 1. Comparison table with previos results

Performace	Process/f_t(GHz)	Frequency (GHz)	Division Ration	Duty-cycle Adjustment	Power (mW)	Supply (V)	Phase Noise @100 kHz (dBc/Hz)	FoM
This work	0.18 μm SiGe/120	0.1-16	1-511	Yes	39	3.3	-153	3.4
Ref [1]	0.18 μm SiGe/200	4.7	16-159	No	10.62	1.8	--	2.2
Ref [3]	90 nm CMOS/120	10-20	2/3	No	0.339	1.2	-137	491
Ref [4]	55 nm CMOS/220	26-44	256-508	No	15.2	1.2	--	13.1
Ref [7]	0.13 μm SiGe/200	0.5-20	1-31	No	264	3.3	-158	0.37
Ref [12]	0.35 μm SiGe/43	1-12	16-(2^{19}-1)	No	--	3.3	--	--

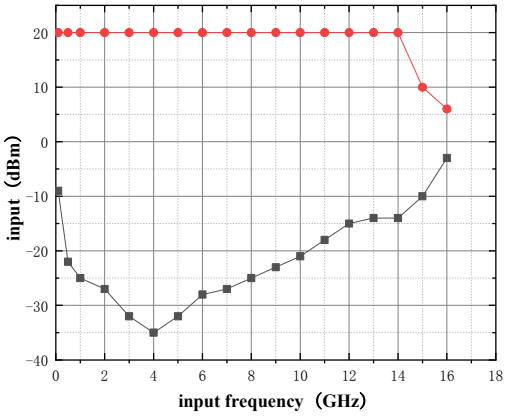
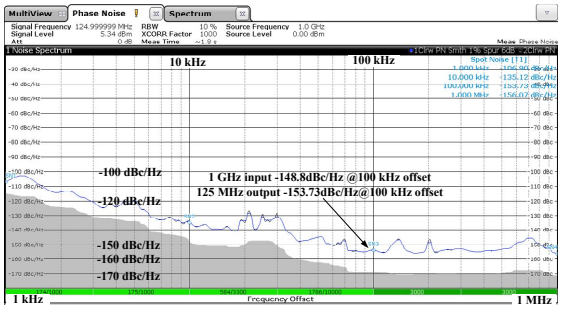


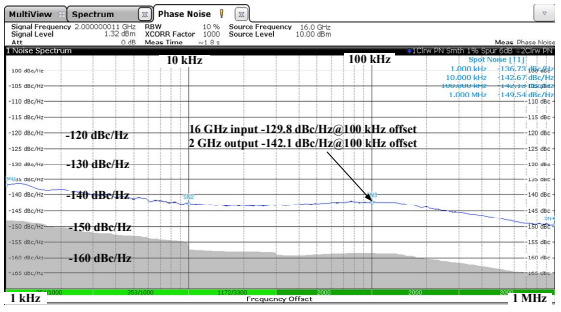
Fig. 10. Test results of input sensitivity @ divide-by-8.

of divide-by-8 and divide-by-511 with the 16 GHz clock frequency. It can be seen from the figure that the output amplitude is greater than 1 Vpp with a 50 Ohm load, and the duty cycle of the output waveform does not show obvious declination in various modes.

The input sensitivity in the mode of divide-by-8 is shown in Fig. 10. In this mode, the circuit can operate correctly with the input power of -20 dBm~+20 dBm. The red dot in Fig. 10 represents the upper limit of the input power for the chip during operation. Exceeding this limit, the internal frequency division link does not work due to excessive signal power, resulting in functional failure. The black dot in the figure represents the lower limit of input power. If the input power is lower than this, the chip cannot process properly and consequently cannot function properly. The chip can operate normally and reliably when the input signal power is between the upper limit curve (red) and the lower limit curve (black). At 4 GHz, it exhibits the lowest input sensitivity due to the fact that the self-oscillation frequency of the first stage divider coincides with this frequency, so only the relatively lowest input power is required to ensure the normal operation of the divider.



(a)



(b)

Fig. 11. Measured phase noise @: (a) 1 GHz; (b) 16 GHz input divide-by-8.

Fig. 11(a) shows the phase noise test of the output signal in the mode of divide-by-8 with the 1 GHz input clock. The results show that the phase noise is better than -153.7 dBc/Hz at the 100 kHz frequency offset. Fig. 11(b) shows the phase noise measurement with an input of 16 GHz in the mode of divide-by-8. The results show that the phase noise is better than -142.1 dBc/Hz with 16 GHz input. The phase noise characteristics of the signal source R&S FSWP at 1 GHz and 16 GHz are -148.8, -129.8 dBc/Hz @ 100 kHz offset, respectively. It is known that the phase noises of both the input signal source and the chip deteriorate with the increase in frequency. When the circuit works at 16 GHz divide-by-8 mode and is tested with the direct method, the phase

noise deterioration of the chip is less than 5.7 dBc. Compared with the existing results, the phase noise results at high frequencies are still excellent.

The total power consumption of the frequency divider core circuit is 39 mW, with a supply voltage of -3.3 V.

The performance of the proposed frequency divider has been compared with existing works and is presented in Table 1. For high-frequency dividers, the following FoM definition is usually used to compare the performance:

$$\text{FoM}=f_{\max}/(\text{Power}\times f_t)$$

where f_{max} is the highest operating frequency of the frequency divider; Power is the power consumption of the divider at the highest operating frequency, and f_t is the cutoff frequency of the device used. Ref [3] and Ref [4] in the table are dynamic frequency dividers, and their operating frequencies cannot cover low frequencies, so they have an advantage in power consumption. The remaining works are static structures so that they can operate from low frequencies to high frequencies. In comparison, the structure presented in this paper can achieve better FoM values. Meanwhile it also has excellent phase noise performance.

V. CONCLUSIONS

This paper proposes an optimized programmable frequency divider that can arbitrarily expand the frequency division ratio. It integrates the high-speed logic operation and reset control in the D flip-flop to realize a high-speed 1-511 continuous integer programmable frequency divider. Its output duty cycle is always close to 50%. The highest operating frequency is 16 GHz, and the lowest sensitivity is better than -30 dBm. The output signal phase noise is -153.7 dBc/Hz @ 100 kHz offset.

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