A Sound Activity Monitor with 96.3 μs Wake-up Time and 2.5 μW Power Consumption

Jinkee Kim, Yunyoung Jang, and Jong Pal Kim

Abstract—A novel low power sound activity monitor (SAM) for fast wake-up is presented. SAM is used for low power consumption of intelligent microphones. An intelligent microphone that responds to user voice commands should operate for 24 hours. Normally, the microphone remains in low power mode when there is no external sound input. While the SAM detects external sound input, the SAM changes from low power mode to normal power mode and the microphone remains in normal power mode. The wake-up time from low power mode to normal power mode should be as short as possible so that user commands are not lost. In addition, power mode switching must be prevented from malfunctioning due to artifacts generated when changing between power modes. Low power and wake-up characteristics are improved by simplifying the SAM structure, and the decision logic is designed to be robust against power switching artifacts. The proposed SAM was designed and fabricated based on a CMOS 0.18 μm process, and its features and performance were measured. The SAM operating at 1.8V consumes 2.5 μW power, and the fast wake-up performance of 96.3 μs is measured.

Index Terms—Microphone, low power, sound activity monitor, wake-up time

I. INTRODUCTION

MEMS technology has replaced a microphone with a MEMS type from a conventional electret condenser (ECM) thanks to the advantages of mass production and miniaturization using a semiconductor process [1]. Subsequently, MEMS microphones are emerging as application examples that are combined with artificial intelligence [2]. Recent great advances in artificial intelligence have brought voice recognition performance to human levels [3].

Intelligent MEMS microphones are turned on 24 hours to recognize user’s voice commands, so power consumption becomes one of key competition factors. A readout integrated circuit (ROIC) can achieve low power consumption by averaging power consumption during long low power mode periods and short normal power mode periods. Most of the time when there is no voice command, the ROIC operates in a low power mode. If an external sound is generated while the ROIC is in low power mode, the ROIC immediately switches to normal power mode. To enable this operating scenario, a SAM that detects external sound in low power mode and controls switching between power modes is required. Therefore, SAMs are required to have extremely low power. Fig. 1 shows an operating scenario for a microphone utilizing SAM. The power mode of a source follower (SF) is controlled according to the output signal (WUP) of the SAM. When there is no sound input, the SAM generates a LOW state in the WUP signal and the SF stays in low power mode. When an external sound input occurs, the SAM outputs a HIGH state signal (WUP) and the SF switches to normal power mode.

It is recommended that the wake-up time from low
power mode to normal power mode should be as short as possible to fully detect the initiation of a user command. Therefore, SAM should quickly detect the voice signal and switch the SF’s power mode. When switching the power mode, it affects the shift of the operating point of the circuit, so the power mode may not switch to the desired mode and return to the previous mode. In the next chapters, a novel SAM circuit is presented to improve issues such as low power, fast wake-up and power mode switching robustness.

II. ARCHITECTURE AND CIRCUITS

Fig. 2 shows the microphone ROIC consisting of a source follower (SF) and a low-power, fast wake-up SAM. SF works as an analog buffer whose power mode is controlled by the WUP signal. When WUP is LOW, SF stands by in low power mode, and operates in normal power mode when WUP is HIGH. SAM consists of open amplifier (OA), 2nd amplifier (AMP2), comparator (CMP), and decision logic circuit (LOGIC). OA and AMP2 amplify the output signal of SF, CMP converts the presence or absence of an AC signal corresponding to sound input into a digital signal, and LOGIC outputs the control signal WUP. In Fig. 2, there are two SFs and they output differential signals (SF(IP)/SF(IN)). If the MEMS transducer is a differential type, all SF inputs (SF(IP)/SF(IN)) are connected to the MEMS transducer, and if the MEMS transducer is a single type, only the SF input SF(IP) is connected to the MEMS transducer and the SF input SF(IN) is connected to a fixed bias.

Fig. 3 shows the detailed circuit diagram of the SF and how it is connected to the MEMS transducer. MEMS transducers can be modeled with a capacitance C_mem, that fluctuates with sound pressure and a fixed parasitic capacitor C_p. When a sound pressure is generated from the outside, an ac voltage signal corresponding to V_m (= V_dr × C_mem/(C_mem + C_p)) is generated. SF analog buffers this V_m voltage.

The input signal SF(IP) is buffered to SF_OP by an MN30 operating as source follower. The SF_IP is connected to V_bf using a PMOS pseudo resistor R_bf to make same the DC voltage as V_bf. In Fig. 3, V_bf is 0.9 V, and R_bf has a value of 146.7 GΩ from simulation. When the WUP...
signal is LOW, only 100 nA of current ($I_{LP}$) flows in the source follower MN30 and the SF operates in low power mode. When the WUP signal is HIGH, 7.6 μA of current ($I_{LP} + I_{NP}$) flows in the source follower MN30 and the SF operates in normal power mode.

The SAM for an intelligent microphone should have low power consumption. For low power and fast wake-up characteristics, the envelope detector used in the conventional SAM structure in the previous work is removed [4].

Fig. 4(a) shows the detail circuit diagram of OA. The OA consists of a high pass filter (HPF), an inverter-based amplifier and common mode feedback. The amplification gain of OA is based on the open-loop type rather than the closed-loop type because the application does not require precise gain. In the case of an open loop type amplifier, compensation is not required to secure stability, so it has advantages in terms of power consumption and area [5, 6].

Fig. 4(b) shows the circuit diagram of AMP2. The AMP2 have charge amplifier structure to remove the DC offset and common-mode signal from OA outputs [7, 8]. The resistors used in the HPF of OA and the feedback loop of AMP2 are adjustable pseudo resistors using the PMOS referenced in [9].

The CMP is designed with positive feedback structure. The CMP makes digital 1 bit signal by comparing the differential output of AMP2. A detailed description of the analog circuits can be found in the author’s previous paper on the design of the SAM [10].

Fig. 5 shows the circuit diagram of LOGIC. SAM should make the WUP signal rising edge when the voice signal occurs to switch the SF to normal power mode. When a rising edge occurs in CMP due to a voice signal, the WUP signal immediately becomes HIGH through D flip-flops (DFF#1, DFF#2).

When no more voice signal is input to the SAM, the WUP signal should go from HIGH to LOW. The WUP signal goes LOW when the low active reset signal (RST_FALLING) resets DFF#2. Low active reset signals are generated in the auto pulse block (AP) when a rising edge occurs on the input. If there is no sound from the outside for a certain period of time, the CALM signal changes from LOW to HIGH, and a reset signal is generated on AP#2 output. When there is a signal change in input signal CMP_out, DIV is continuously reset by AP#1 and output CALM maintains LOW state. If there is no more signal change in the input signal CMP_out, DIV is no longer reset and the output value is converted from LOW to HIGH after and certain period of time ($T_{\text{wait}}$). The $T_{\text{wait}}$ time can be adjusted by register setting.

At the moment WUP transitions from HIGH to LOW, the current flowing through SF decreases, causing the output DC value to step up. This DC step in SF acts as an artifact, leading to false positive detection of sound. This artifact changes the power mode back to the normal power mode, and thus falls into an infinite circulation loop in the normal power mode. Therefore, after WUP changes from HIGH to LOW, DFF#1 responds to the input signal CMP_out after half cycle of CLK. DFF#1 does not transfer CMP_out change to output until it is reset by EN_INPUT signal. The EN_INPUT signal is generated by combining the CALM signal and the CLK signal.
Fig. 6. Fabricated chip photograph.

Fig. 7. Measured analog characteristics: (a) Frequency response; (b) Input referred noise of SF, OA, and AMP2.

III. MEASUREMENT RESULTS

Fig. 6 shows a picture of a chip fabricated based on the CMOS 0.18 μm process. Regions corresponding to blocks in the schematic are indicated by rectangular boxes.

Fig. 7(a) shows the frequency response of the SF, OA, and AMP2. The SF has a bandwidth of 5.2 kHz in low power mode and 35.3 kHz in normal power mode. The OA block has a high-pass cutoff frequency of 2.1 Hz, a low-pass cutoff frequency of 1.7 kHz and a peak gain of 44 dB (158.5 V/V) at 100 Hz. The AMP2 block has a high-pass cutoff frequency of 1.5 Hz, a low-pass cutoff frequency of 3.1 kHz, with a peak gain of 19.5 dB (9.4 V/V). Therefore, the overall gain of the analog amplifiers (OA + AMP2) is 63.5 dB. The output signal of AMP2 may be saturated when a large input signal is supplied to the SAM. However, since SAM detects only the presence of sound, it does not matter even if the signal is saturated. Since the audio signal is an ac type signal, the saturated signal will be in the form of a digital clock, and in this case, it will be a more favorable condition for detecting the presence or absence of sound in the comparator and logic.

Fig. 7(b) shows the noise characteristics of the combined blocks of SF, OA and AMP2. Input referred noise at 1 kHz has 351.4 nVrms/√Hz in low power mode and 277.8 nVrms/√Hz in normal power mode.

Fig. 8 shows the signals of successive blocks (SF, OA, AMP2, and CMP) and the WUP signal of LOGIC block. When EN_SOURCE is HIGH, a sinusoidal signal with a magnitude of 150 μVpk and a frequency of 1 kHz was fed to the SF input. While the sinusoidal wave input is applied from time $t_1$ to time $t_2$, the successively amplified differential output signal $OAPK$ of OA and the differential output signal $AMP2OPK$ of AMP2 can be seen. It can also be seen that LOW and HIGH signals appear at the comparator output $CMP_{OUT}$ in response to the amplified analog signal. As soon as the input signal appears, it can be verified that the WUP signal changes from LOW to HIGH at time $t_i$. As the WUP signal goes HIGH, the SF operates in normal power mode, and it can be seen that the operation DC level of $SF_{OP}$ changes at $t_i$. 
This is caused by the increased current flowing in the SF block. The sinusoidal input is cut off at $t_2$ and the WUP signal goes LOW at $t_3$ after a $T_{\text{wait}}$ period. Since command input may be interrupted for a while depending on syllables and words, it is necessary to wait for $T_{\text{wait}}$ without changing the power mode even if there is no sound for a while.

As $WUP$ changes from HIGH to LOW at time $t_3$, it can be seen that the output value $SF_{\text{up}}$ of SF steps up. This is because the flowing current of SF is reduced from 7.6 μA to 100 nA as the SF switches from normal power mode to low power mode. This SF output step signal change is amplified and transmitted to the input signal of LOGIC, causing a false recognition reaction as if external sound was re-input. In order to prevent the $WUP$ signal from malfunctioning from these artifacts, the LOGIC input was enabled after half a clock cycle after the $WUP$ signal falling edge. Since the anti-artifact function is implemented, we can see that $WUP$ signal does not bounce back to HIGH and $WUP$ stays LOW at $t_3$.

Fig. 9 shows the wake-up time of the ROIC. When a signal is input to the SF, the wake-up time $T_{WUP}$ is the sum of the time interval $T_{\text{sense}}$ and the time interval $T_{\text{set}}$. A 1 kHz, 3 mV pk sine waveform is input to the SF to measure the wake-up time. The time interval $T_{\text{sense}}$ is the time consumed for $WUP$ to become HIGH after the signal is input. The time interval $T_{\text{sense}}$ was measured as 61.3 μs. The time interval $T_{\text{set}}$ is the time it takes for the SF to switch power modes and output signals to reach 90% of the input signal. The time interval $T_{\text{set}}$ was measured as 35 μs.

In Table 1, the performance of the proposed SAM is summarized and compared with previous work. The proposed SAM aims at fast wake-up and achieved a wake-up time of 96.3 μs, which is much faster than the existing wake-up time of 760 μs to 4 ms. In reference [4], Yang uses two envelope detectors for the anti-artifact function, so the wake-up time is as slow as 4 ms and the power consumption is 8.3 uW. On the other hand, in this paper, the wake-up time was reduced to 96.3us and power consumption to 2.5 uW because the anti-artifact function was handled by LOGIC without an envelope detector. In addition, an active mode hold function has been added to suppress frequent power mode changes by considering short breaks between syllables as command end.

### IV. Conclusion

A low power, fast wake-up SAM with a novel structure is proposed. SAM reduces the average temporal power consumption of ROIC by controlling the power of the main channel according to the presence or absence of sound. Low power consumption was realized by removing the envelope detector in the previous structure, and artifacts were overcome by using comparator’s hysteresis characteristics and LOGIC. The ROIC using the proposed SAM was fabricated with a standard CMOS 0.18 μm process and verified through functional and performance measurements. The total gain and noise of the analog amplifier (OA + AMP2) measured 63.5 dB and 351.4 nV/√Hz respectively at 1 kHz in low power

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Fabrication technology</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>SAM power (current) consumption</td>
<td>2.5 μW (1.4 μA)</td>
<td>8.3 μW (2.5 μA)</td>
<td>46.2 μW (14 μA)</td>
</tr>
<tr>
<td>Wake-up time</td>
<td>96.3 μs</td>
<td>4 ms</td>
<td>760 μs</td>
</tr>
<tr>
<td>Chip Area</td>
<td>2.5 mm²</td>
<td>3.7 mm²</td>
<td>3.1 mm²</td>
</tr>
<tr>
<td>Anti-artifact</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Active mode holding</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
</tbody>
</table>
mode. The power consumption and wake-up time of the fabricated SAM were measured as 2.5 μW and 96.3 μs, respectively. In addition, it was confirmed that the proposed immune function works well in response to power mode change artifact.

ACKNOWLEDGMENTS

This paper was supported by Education and Research promotion program of KOREATECH in 2021. This paper was supported by "Leaders in Industry-university Cooperation 3.0 (1345356194)" project grant funded by the Ministry of Education and the National Research Foundation of Korea (LINC3.0-2022-31). The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

This paper was supported by Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) (P0008458, The Competency Development Program for Industry Specialist, 2023).

REFERENCES


Jinkee Kim received his B.S. degree in Mechatronics Engineering from Korea University of Technology and Education, Cheonan, Korea, in 2021, where he is currently pursuing M.S. degree. His research interests include low power bio-applicable circuit.

Yunyoung Jang received his B.S. degree in Mechatronics Engineering from Korea University of Technology and Education, Cheonan, Korea, in 2021, where he is currently pursuing M.S. degree. His research interests include low power bio-applicable circuit.
Jong Pal Kim received his B.S. degree in mechanical design from the Department of Mechanical Design, Chung-Ang University, Seoul, Korea, M.S. degree in mechanical engineering from KAIST, Daejon, Korea, and Ph.D. degrees in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 1995, 1997, and 2003, respectively. He was a member of research staff at Samsung Advanced Institute of Technology (SAIT) from 2001 to 2019. In 2020, he joined the Faculty of School of Mechatronics Engineering, Korea University of Technology and Education, Cheonan, Korea. His research interests include low power and low noise analog integrated circuits for biomedical and MEMS applications.