JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL. 24, NO. 4, AUGUST, 2024
https://doi.org/10.5573/JSTS.2024.24.4.289
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A Fast Settling, 0.1-100% Duty-cycled, 1-100 mA Accurate Current Control LED Driver for PPG Sensor System

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***Abstract*—A wide operating range, fast settling, and accurate current sourcing LED driver for PPG (Photoplethysmography) sensor applications is presented. Proposed NMOS resistor array and RC-time constant based calibration circuit precisely control target LED driving current with less than 0.5% error over process variations. For the fast settling of pulse-width modulation (PWM) based boost converter loop, pulse-width prediction technique is proposed which greatly improves the settling time. The driver circuit is designed in 180-nm CMOS process, supporting green/red/infrared LED driving voltage, 0.1-100% duty-cycling and 1-100 mA driving current.**

***Index Terms*—LED driver, PPG sensor, current calibration, fact settling, boost converter**

I. INTRODUCTION

Photoplethysmography (PPG) is a method that can detect the changes in blood volume inside capillary vessels by measuring reflected or transmitted light among the light irradiated on the human body. PPG can non-invasively measure heart rate or blood oxygen saturation, so it is widely used in medical devices and wearable sensors.

Manuscript received Oct. 9, 2023; reviewed Mar. 13, 2024; accepted Apr. 29, 2024
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LED is generally used to irradiate light to the human body in PPG applications. LED driver generates the LED forward driving voltage that varies depending to the target brightness of the LED. In general, the following features are required for LED drivers for PPG applications. First, the drivers should control the current accurately, typically in the range of a few mA to 100 mA for closed-loop operation with a readout circuit [1]. Therefore, a calibration circuit for accurate current generation is essential [2]. A DC-DC conversion circuit is often required to generate various optimal turn-on voltages of the LEDs, which varies depending on LEDs' output spectrum. This is because various LED lights such as red, green, and infra-red are used depending on the target PPG application [3, 4]. Finally, duty-cycling of the LED driving is also essential since the LED driver is the dominant source of the power consumption in the PPG system [5].

However, to date, LED drivers for PPG systems have usually been implemented with simple circuits such as voltage drivers [6] or current sources [7-9] only. These drivers adjust the current level or duty-cycle with control signals from readout circuits, but they require several separate high supply voltages to drive various LEDs.

In this paper, we present a high-efficiency LED driver for PPG applications that meets previously mentioned requirements. For the current calibration, we propose NMOS resistor array and RC-time constant based calibration technique. Pulse-width (PW) prediction technique is also proposed which improves the settling time of the boost converter, eliminating unnecessary power consumption during the loop settling. The article is organized as follows. Section II describes the proposed

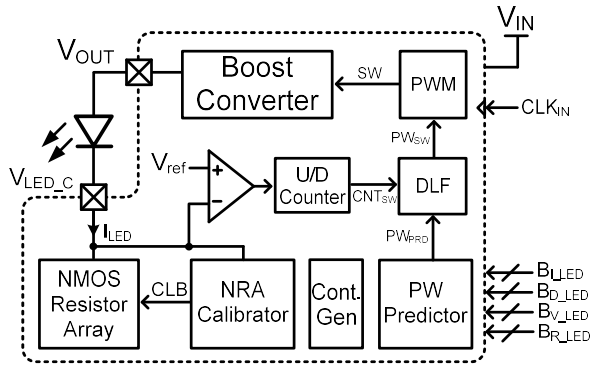

Fig. 1. Top structure of the proposed LED driver.

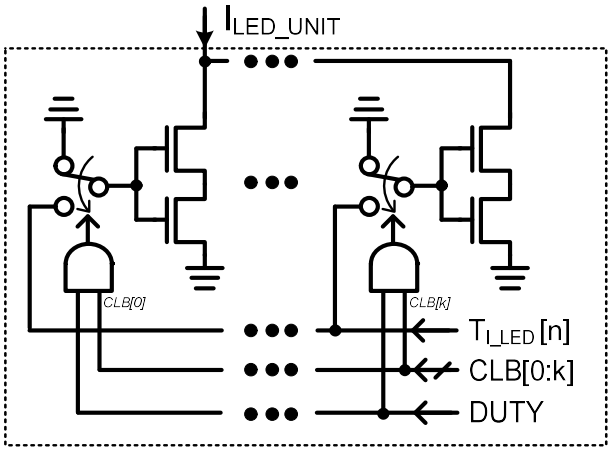

Fig. 2. Unit cell of NMOS resistor array.

driver circuits. Section III presents simulation results and section IV concludes this paper.

II. CIRCUIT DESCRIPTION

1. The Proposed LED Driver Circuit

Top diagram of the proposed driver is shown in Fig. 1. First, NMOS resistor array (NRA) generated LED current I_{LED} whose dc quantity is defined by the control signal B_{I_LED} and whose duty-cycle is defined by the control signal B_{D_LED}. The current control is performed in all-digital way by adjusting the number of NMOS resistors in the array. The current calibration code (CLB) is provided by the NRA calibrator which detect the process variation of the circuit.

The PWM based boost convertor keeps V_{LED_C} to V_{ref} by the closed loop operation and generates V_{OUT} which is determined by the I_{LED} and the LED's I-V characteristics. The control loop consists of a comparator, counter, digital loop filter (DLF) and pulse-width modulation (PWM) signal (SW) generator. PW predictor initializes PWM control code (PW_{SW}) by calculating its initial code (PW_{PRD}) with control inputs (B_{I_LED}, B_{D_LED}, B_{V_LED}, and B_{R_LED}) with proposed PW prediction technique. B_{V_LED} and B_{R_LED} are turn on voltage and equivalent resistance of LED, respectively, which are typically obtained from the LED datasheet.

2. NMOS Resistor Array & Calibrator Circuit

Conventional current control circuit adopts digital-to-analog converter (DAC) [9] and reduces power consumption of current DAC by taking high current amplification ratio with large output driving transistor. However, the output transistor experiences a larger V_{GS} change with wider output current range, and necessarily needs a high V_{DS} to remain in a saturation region. In addition, the duty-cycling of the current sources needs additional settling time for analog node voltages.

In this work, we use NMOS transistor as a resistor for direct output driving current generation. The unit cell of NRA is shown in Fig. 2. The unit cell consists of $k+1^{th}$ stacked NMOS transistors and control logics. Stacked transistor minimizes the area consumption while achieving high resistance for a precise current control. The calibration code CLB[0:k] adjusts the number of NMOS transistors turned on so that the current flowing from each unit cell is 1 mA. DUTY signal is LED duty-cycling signal based on B_{D_LED} input, and collectively turns on and off all the NMOS resistors selected with CLB. One digit of T_{I_LED} controls one unit cell, and a total of 100-unit cells are used to generate 1-100 mA current.

The proposed all digital control not only eliminates static power consumption for LED current generation but also facilitate accurate duty-cycle control. In addition, since the V_{LED_C} is fixed to V_{ref}, the power efficiency is maximized by minimizing the V_{DS} of the transistors regardless of the change in I_{LED} or LED turn-on voltage.

The NRA calibrator circuit and its timing diagram are shows in Fig. 3 and 4. V_{LED_C} is sampled in the C_{CLB} with SPL signal and discharged through NRA replica with DSC signal. NRA replica is designed to draw five times smaller current than NRA unit cell to reduce power consumption. Then the capacitor voltage V_{CLB} and V_{CLB_REF} are compared with the rising edge of SEN with a clocked

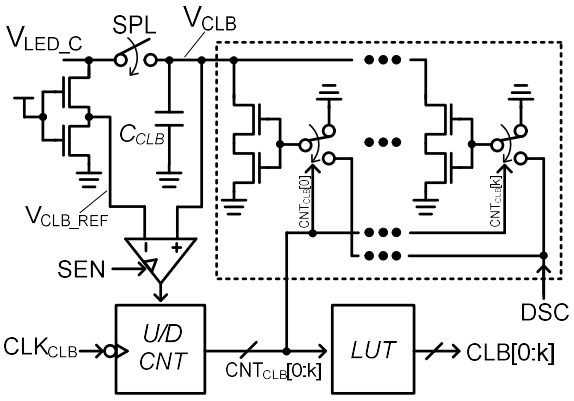

Fig. 3. NRA calibrator.

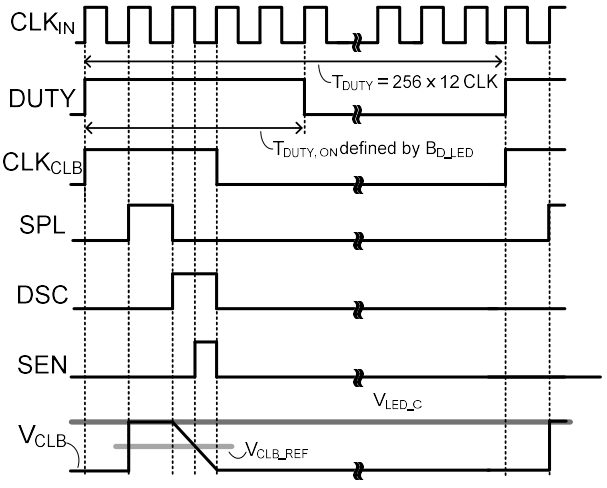

Fig. 4. Timing diagram of NRA calibrator.

comparator. Therefore, RC-discharging time defined by C_{CLB} and NRA replica is compared to the half clock period($1/2 \cdot T_{CLK^{IN}}$), and the NRA resistance variation can be extracted.

However, the comparison result also includes the impact of process variation of C_{CLB}. We adopt the look-up table (LUT) to remove it. First, the comparator output is integrated to up/down counter and its k+1 most significant bits (MSBs) are used for CNT_{CLB}. Then, LUT translates CNT_{CLB} to final NRA calibration code CLB. Fig. 5 shows the CNT_{CLB}-CLB transfer curve for the LUT. It was designed by linearly approximating each of the 5 process corners simulation results.

3. Boost Converter

Fig. 6 shows designed inductor-based boost converter circuit. The CMOS controlled rectifier (CCR) and level

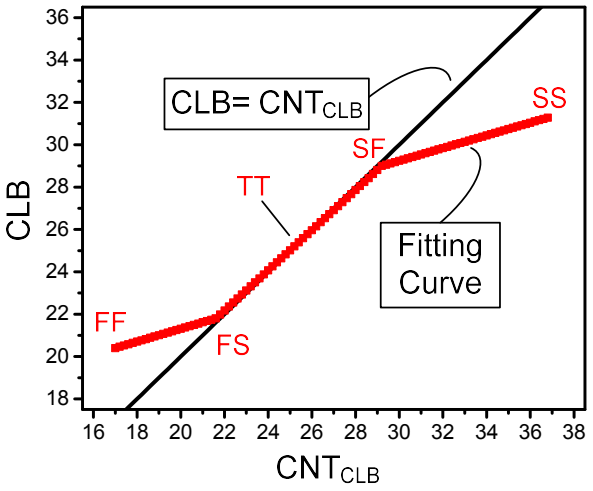

Fig. 5. Fitting curve for LUT design.

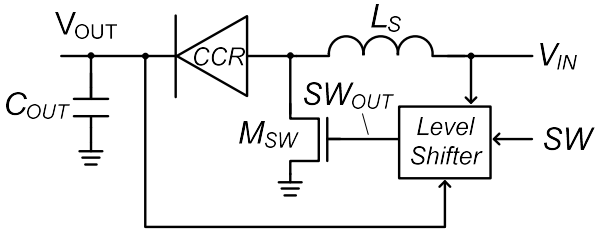

Fig. 6. Circuit diagram of the boost converter.

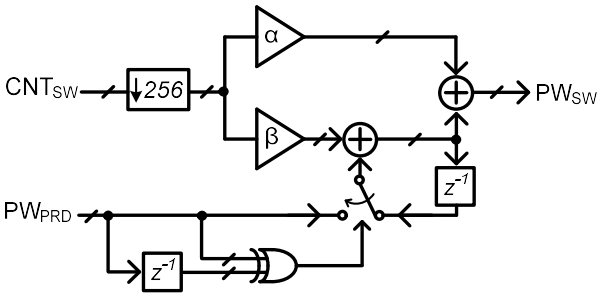

Fig. 7. Circuit diagram of the digital loop filter.

shifter are used to increase power efficiency of the converter [10]. External inductor of 5 μH is used for L_S whose series resistance is 18.4 mΩ (Bourns, SRR6040A5R0Y). External capacitor of 200 μF is used for C_{OUT} to minimize the change in I_{LED} due to V_{OUT} ripple to within 1%. Therefore, since the minimum average I_{LED} is 1 μA at 1 mA output current and 0.1% duty, the required DLF bandwidth for stability should be very low, because of the low frequency output pole at V_{OUT}, which significantly increases the settling time.

The circuit diagram of the DLF is shown in Fig. 7 The proposed PW predictor, which will be described in the

next section, provide calculated target pulse width (PW_{PRD}) for the fast settling. Since the integrator value of DLF should be overwritten with PW_{PRD} only when there is a difference from the target value, whether to update the integrator value is determined by comparing the current and past PW_{PRD}. Loop filter output PW_{SW} has 8-b resolution and the period of the PWM switching signal SW (T_{SW}) is $256\times T_{CLKIN}$.

The proportional gain α and the integral gain β of the DLF can be determined as follows. First, the control-to-output transfer function $G_{vd}(s)$ can be obtained by setting the input voltage change $\widehat{v_{in}}(s)$ to zero and solving the transfer function from the change $\hat{d}(s)$ of the duty cycle of SW_{OUT} to the output voltage change $\widehat{v_{out}}(s)$ [11].

$$G_{vd}(s)=\left.\frac{\widehat{v_{out}}}{\hat{d}}\right|_{\widehat{v_{in}}=0}=\frac{G_{d0}}{1+\frac{s}{\omega_p}} \tag{1}$$

$$G_{d0}=\frac{2V_{OUT}}{D}\frac{M-1}{2M-1} \tag{2}$$

$$M=\frac{1+\sqrt{1+4R_{LED}/R_e}}{2} \tag{3}$$

In (2) and (3), D is the duty cycle of SW_{OUT}, R_{LED} is the load resistance, and R_e is the effective resistance of M_{SW}. The designed boost converter operates in discontinuous conduction mode (DCM). In DCM, the voltage conversion ratio of the boost converter is a function of the switch's operating duty ratio, switching period, inductance, and load resistance [11]. The relationship between the current and voltage of an LED can be expressed by the following equation [13]:

$$I_F=I_s\left(e^{V_F/kT}-1\right) \tag{4}$$

To derive the load resistance, LED is modeled as a resistor R_{LED} with a turn-on voltage V_{on} as follows.

$$R_{LED}=\frac{V_F}{I_F+I_s}\times\frac{1}{\ln\left(I_F/I_s+1\right)} \tag{5}$$

$$V_{on}=V_F-I_F R_{LED} \tag{6}$$

In (4), I_S, V_F and I_F are the reverse bias saturation current, forward voltage and forward current specified in the LED's datasheet, respectively.

Lastly, due to the large capacitance of the output stage, it is considered as a 1-pole system, and the pole frequency (ω_p) can be calculated by the following equation.

$$\omega_p=\frac{2M-1}{(M-1)R_{LED}C_{OUT}} \tag{7}$$

Therefore, the parameters α and β can be obtained by taking the bilinear transform [12] in the continuous time Eq. (1).

4. PW Predictor

The M_{SW} turn-on time ($T_{SW,on}$) for the PWM control of the boost converter is determined by the load current (I_{LED}) and the output voltage V_{out}. I_{LED} are obtained from the control input B_{I_LED}. V_{OUT} is derived as

$$V_{OUT}=V_{LED\_C}+V_{ON}+I_{LED}\cdot R_{LED} \tag{8}$$

V_{LED_C} is converged to V_{ref} with the loop operation, and V_{ON} and R_{LED} are obtained from the control input B_{V_LED} and B_{R_LED}. Therefore, by analyzing the boost converter operation, target $T_{SW,on}$ at a given operating point can be calculated and used for the fast settling of the loop.

$T_{SW,on}$ calculation process is as follow: First, since the voltage across the inductor when the switch is turned on in the boost converter operation is input supply voltage V_{IN}, the maximum current $i_{L,max}$ flowing through the inductor is derived as follows.

$$i_{L,max}=V_{IN}T_{sw,on}/L_S \tag{9}$$

In (9), L_S is the inductance of the inductor. If the voltage across the inductor when the switch is off is V_{OUT}-V_{IN}, and the time taken for the inductor to be completely discharged when the switch is off is $T_{sw,off}$, the following equation can be derived.

$$i_{L,max}=(V_{OUT}-V_{IN})T_{sw,off}/L_S \tag{10}$$

Combining (9) and (10), we get:

$$T_{sw,off}=V_{IN}T_{sw,on}/(V_{OUT}-V_{IN}) \tag{11}$$

The switch M_{SW} operates only when the LED is turned-

on, which is defined by NRA turn on time ($T_{DUTY,on}$) for LED duty-cycling defined by the control input B_{D_LED}. Therefore, during one cycle of DUTY, the M_{SW} operates n times, The n should be integer and is calculated as follows.

$$n = T_{DUTY,on} / T_{sw} \fallingdotseq T_{DUTY,on} / T_{sw} + 1 \tag{12}$$

Therefore, the input average power ($P_{IN,avg}$) is derived as:

$$P_{IN,avg} = \frac{V_{IN} \times n \times i_{L,max} \times \left(T_{sw,on} + T_{sw,off}\right)}{2T_{DUTY}} = \frac{V_{IN}{}^2 \times n \times T_{sw,on}{}^2}{2L_S T_{DUTY}} \times \frac{V_{OUT}}{V_{OUT} - V_{IN}} \tag{13}$$

And the output average power ($P_{OUT,avg}$) is:

$$P_{OUT,avg} = V_{OUT}\left(I_{LED}\frac{T_{DUTY,on}}{T_{DUTY}} + I_{DC}\right) \tag{14}$$

In (14), I_{LED} is the LED current and is defined by the control input B_{I_LED}. I_{DC} is a dc biasing current for CCR and level shifter in the boost converter, which is obtained from SPICE circuit simulations. T_{DUTY} is the period of the LED duty-cycling ($12\times256\times T_{CLK_{IN}}$). Finally, assuming that the average power supplied through the inductor L_S and the power dissipated from V_{OUT} are the same, (13) and (14) are equal, we obtain $T_{SW,on}$ as follow

$$T_{sw,on} = \sqrt{\frac{2 \cdot L_S \cdot T_{DUTY} \cdot T_{SW}}{\left(T_{DUTY,ON} + T_{SW}\right) \cdot V_{IN}^2}} \times \sqrt{\left(V_{OUT} - V_{IN}\right) \cdot \left(I_{LED}\frac{T_{DUTY,ON}}{T_{DUTY}} + I_{DC}\right)} \tag{15}$$

PW predictor performs digital signal processing of the Eq. (15) from control input ($B_{I\_LED}\rightarrow I_{LED}$, $B_{D\_LED}\rightarrow T_{DUTY\_ON}$, B_{V_LED} and $B_{R\_LED}\rightarrow V_{OUT}$) and circuit design parameters (L_S, V_{IN}, I_{DC}, T_{DUTY}, T_{SW}). Processed output is 8-b PW_{PRD} code, which generates $T_{SW,on}$ of $PW_{PRD} \times T_{CLK_{IN}}$.

III. Implementation and Results

Proposed driver circuit is designed with 180-nm CMOS process. Digital signal processing circuits including DLF and PW predictor are implemented with digital synthesis.

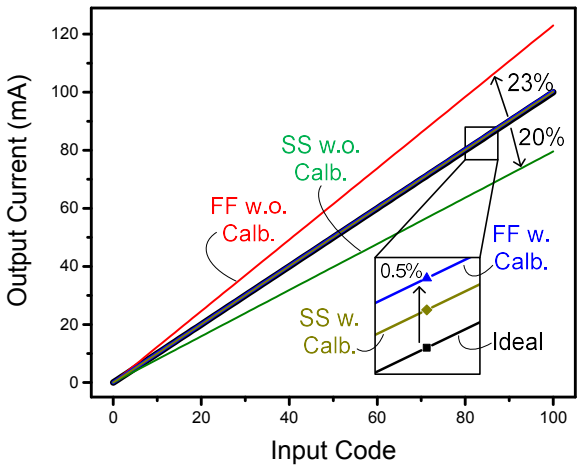

Fig. 8. Output current accuracy over process variation.

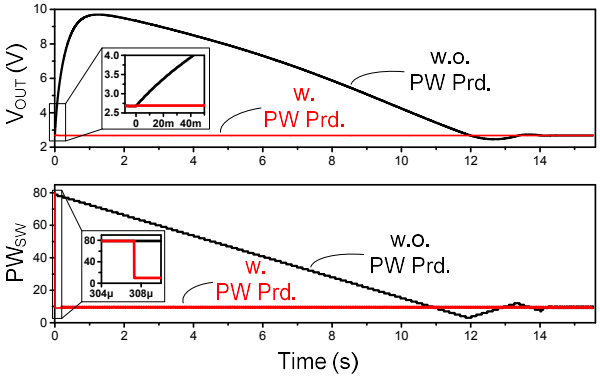

Fig. 9. Transient simulation results of boost converter.

For the simple digital circuit implementation, we use the repeated subtraction method [14] for the square root operation. Maximum simulated efficiency is 89% at 100 mA, 100% duty with green LED (Osram, LGT676). From the LED datasheet and the Eqs. (5) and (6), V_{on} and R_{LED} are calculated as 1.84 V and 13 Ω, respectively. The supply voltage (V_{IN}) is 1 V. For CLK_{IN}, 10 MHz is used. V_{ref} is set to 200 mV. Output voltage (V_{OUT}) is 1.3-4.5 V with an input voltage (V_{IN}) of 1 V through boost converter control.

Fig. 8 shows simulated output current over process variation. The result shows the maximum current error is 23% at FF corner, but it is improved to less than 0.5% with the proposed calibration technique.

Fig. 9 shows the transient simulation result with 100 mA I_{LED} and 100→0.1% duty change at t=0. It takes unacceptably long time for V_{OUT} to be settled without the proposed technique, because the PW_{SW} slowly decreases due to the low loop bandwidth while the power

Table 1. Performance comparison (LED driver for PPG)

	[15]	[16]	[17]	This work
Technology	0.18 μm	0.18 μm	0.13 μm	0.18 μm
Supply Voltage	1.2/3.3 V	1/2.5 V	1.5/2.7 V	1 V
LED Current	5 mA	0.1-103.2 mA	50 mA	1-100 mA
LED duty cycle	1%	10.24%	1%	0.1-100%
Current Calibration	N.A.	No	No	Yes
Integrated DC-DC Converter	No	No	No	Yes (w. Fast Settling)

Table 2. Performance comparison (DC-DC converter)

	[10]	[18]	[19]	This work
Technology	0.35 μm	0.35 μm	0.5 μm	0.18 μm
Supply Voltage	0.9-1.2 V	6-27 V	3.5-5 V	1 V
Clock Frequency	667 kHz	39 kHz	2 MHz	10 MHz
Maximum Efficiency	87%	90%	90.7%	89%

consumption in the LED is dropped by 1/1000 with the duty change. By the proposed PW prediction technique, PW_{SW} code is immediately changed from 79 to 10 and the settling time of V_{out} (<0.1% error) is greatly improved from 14.307 s to 124 ms.

Tables 1 and 2 summarize the performance of the proposed LED driver for PPG and compare it with previously published LED drivers and DC-DC converters. The proposed LED driver is the only work that integrates several essential features for PPG applications, a wide-range duty cycling, accurate current control and DC-DC converter supporting various types of LEDs. The power efficiency of the boost converter is also comparable to other state of the art works.

IV. CONCLUSIONS

A 0.1-100% duty-cycled, 1-100 mA, 89% efficiency LED driver for PPG application is presented. Proposed current generation using digitally controlled NRA facilitates duty-cycle control, and the RC-time based calibration technique reduces current error over process variations to less than 0.5%. The PW predictor calculates required pulse-width corresponding the given load condition, and greatly improves the settling time even with the low loop bandwidth of wide operating range boost converter.

ACKNOWLEDGMENTS

This research was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT(RS-2023-00258227). The EDA tools were supported by IDEC.

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