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# Work-Function Variation and Delay Analysis in NAND and NOR Circuits using Gate Insulator Stack-based Dopingless Tunnel Field-effect Transistors

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***Abstract*—This paper investigates the electrical characteristics of work-function variation (WFV) in dopingless Tunnel Field-Effect Transistor (TFETs) with $SiO_2$-$Si_3N_4$-$SiO_2$ (ONO) gate insulator stacks. It explores the potential benefits of using ONO structures to mitigate WFV's impact on the channel. The study also examines the immunity of TFETs to WFV and current variations compared to doping-based junctions. The paper begins by discussing the challenges introduced by increased doping concentrations, specifically poly/metal-grain granularity (MGG). The proposed dopingless TFET with an ONO stack structure is introduced, acknowledging the need for rigorous validation. Detailed information on device simulation and programming sequences for TFETs is provided. The mixed-signal circuit configuration is outlined, focusing on the use of high-performance MOSFETs and TFETs to enhance output voltage margins and reduce transition time variations. The study concludes by presenting the electrical characteristics of WFV and its impact on TFET devices. The effectiveness of program adjustments in reducing threshold voltage ($V_t$) scatter for both n-type and p-type TFETs is discussed. In summary, this study explains the advantages and limitations of dopingless TFETs with ONO stack structures, offering insights into their application.**

***Index Terms*—TFET, ONO, WFV**

## I. INTRODUCTION

For many decades, there has been a continuous effort to enhance the electrical performance of metal-oxide-semiconductor field-effect transistors (MOSFETs) in low-power applications, primarily through the adoption of FinFET or gate-all-around (GAA) structures [1-5]. However, these structures do not enable steep switching in transfer curves due to a theoretical limit of 60 mV/decade subthreshold swing (SS) caused by the Boltzmann tail in the source region. To address this challenge, tunnel field-effect transistors (TFETs) have been investigated to eliminate the Boltzmann tail and achieve SS values below 60 mV/decade [6-19]. This extremely low SS indicates very low static power consumption, which can lead to significant performance improvements in low-speed applications. For example, MAC (Multiply-Accumulate) units require high computational throughput with low power consumption,

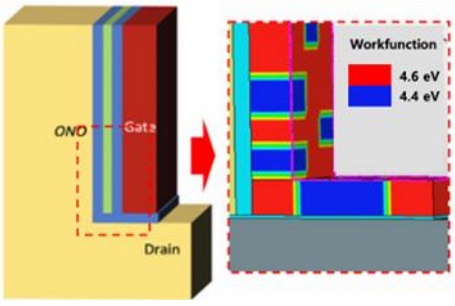


**Fig. 1.** Structure of the doping-less tunnel field-effect transistor (TFET) with charge trap layer.

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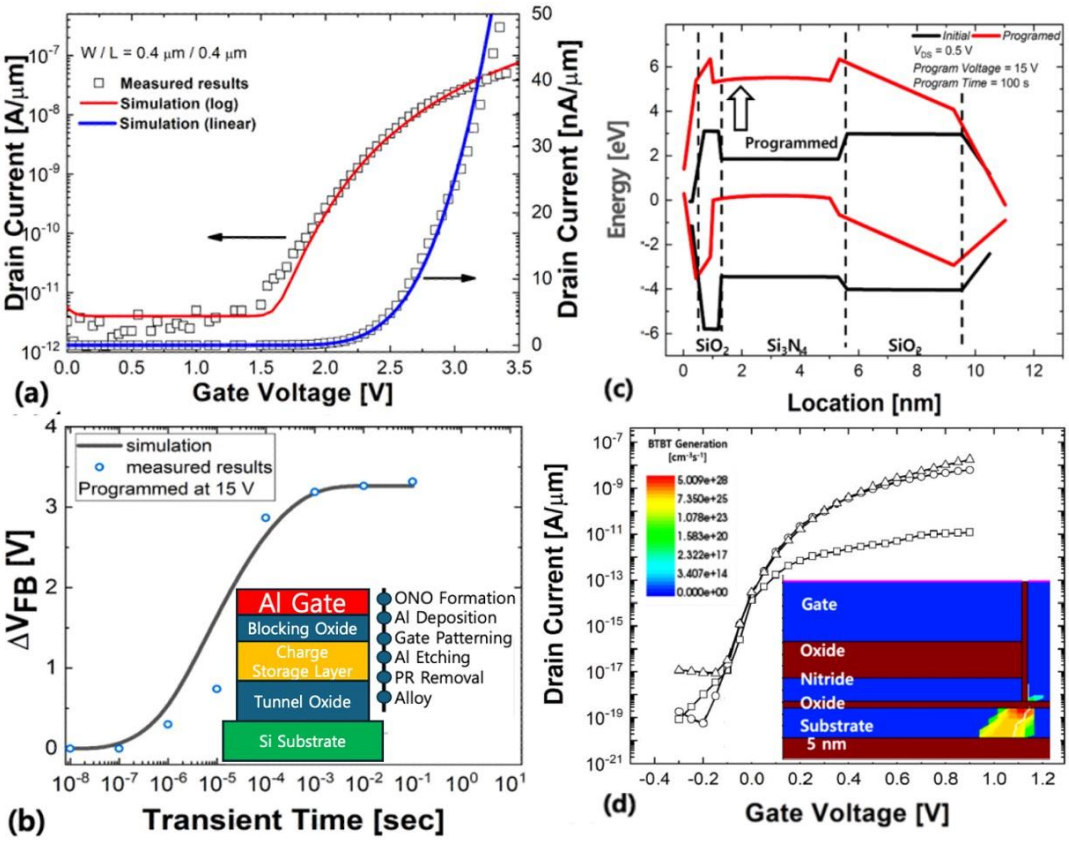



**Fig. 2.** Structure of the doping-less tunnel field-effect transistor (TFET) with charge trap layer.

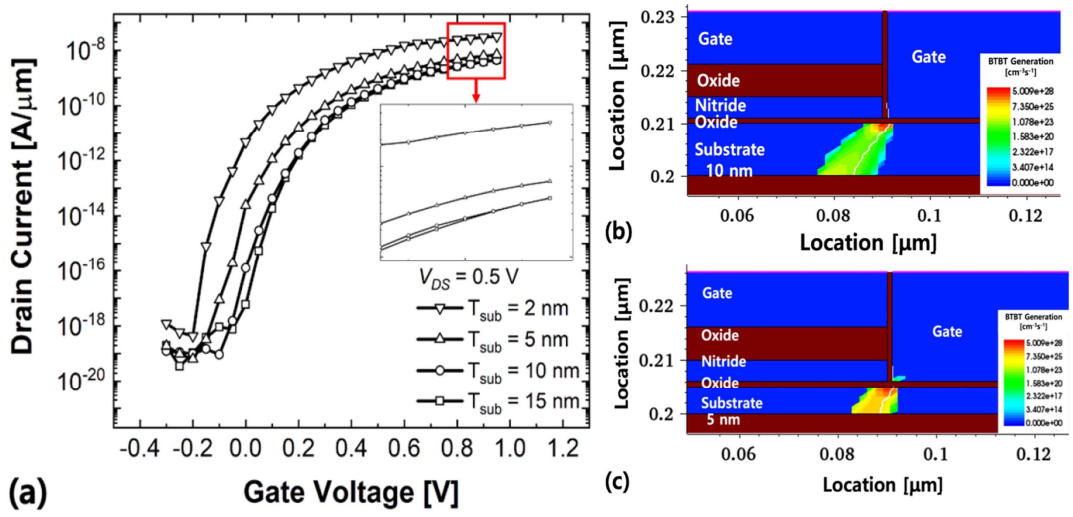



**Fig. 3.** (a) Transfer curves of proposed TFET. BTBT generation rate on the source region; (b) 10 nm; (c) 5 nm of substrate thickness.

making this device suitable for such applications [20].

Furthermore, as MOSFETs have scaled down to the nanoscale, the doping concentration in the MOSFET channel has increased to enhance the gate's control over the channel. However, this increase in doping concentration has introduced issues such as poly/metal-grain granularity (MGG). These variations make it challenging to produce integrated circuit chips with a high yield during the manufacturing process [16-19].

To address these challenges, doping-less TFETs that operate by forming an energy band using the charge trap within the gate insulator has been studied. The gate

**Table 1.** Parameters of TCAD simulation

| Parameters | Material / Dopant | Values |
|---|---|---|
| Bottom oxide thickness | $SiO_2$ | 1 nm |
| Top oxide thickness | $SiO_2$ | 6 nm |
| Nitride thickness | $Si_3N_4$ | 2 nm |
| Body contact doping | Si / p-type | $5 \times 10^{18}$ cm$^{-3}$ |
| Drain doping concentration | Si / n-type | $5 \times 10^{18}$ cm$^{-3}$ |
| Channel doping concentration | Si / p-type | $1 \times 10^{15}$ cm$^{-3}$ |
| Channel length | - | 60 nm |

insulator of the proposed device consists of a triple dielectric stack (ONO: $SiO_2$-$Si_3N_4$-$SiO_2$). Electrons trapped in the nitride layer of the ONO dielectric form an energy band between the source and the channel. When considering work function variation (WFV) related to metal grain, it is expected that there is no immunity against current variations compared to junctions formed by doping. However, this immunity is not confirmed and needs rigorous validation [17-19].

In this paper, we investigate the electrical characteristics of WFV in a dopingless TFETs with an ONO stack. When employing the ONO structure and ONO programming, it is anticipated that the impact on the channel will be reduced, even in the presence of WFV.

## II. DEVICE SIMULATION

The device configuration of the charge trap TFETs employed in this simulation is illustrated in Fig. 1. The ONO dielectric layers are comprised of $SiO_2$, $Si_3N_4$, and $SiO_2$. The thickness of the bottom oxide layer ($T_{OXB}$) is 1 nm, the top oxide layer ($T_{OXT}$) measures 6 nm, and the nitride layer ($T_N$) is 2 nm thick. All source, drain, and channel materials are made of silicon (Si). To mitigate the impact of the short channel effect (SCE), the channel length ($L_{Channel}$) is set at 60 nm. There is no doping in the tunnel barrier that carries the current. However, doping has been introduced in the source region to reduce contact resistance. The body contact doping ($N_S$) is $5\times10^{18}$ cm$^{-3}$ (p-type), drain doping ($N_D$) is $5\times10^{18}$ cm$^{-3}$ (n-type), and body doping ($N_{sub}$) is $1\times10^{15}$ cm$^{-3}$ (p-type). We have placed a p+ region behind the source area to facilitate the smooth charge/discharge of holes. This p+ region does not need to be added to each device individually; it can be shared among multiple devices.

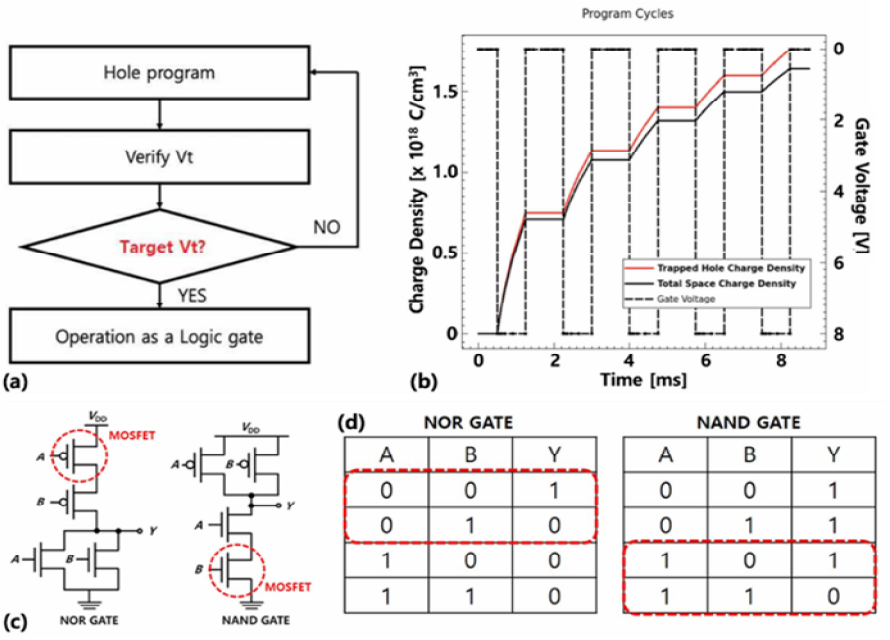
The material employed in the WFV model was TiN, with WFV values of 4.4 eV and 4.6 eV, each representing 40 % and 60 % probabilities, randomly distributed on the gate. A total of 50 samples were produced for each simulation run and subsequently assessed. The characteristics of the doping-less TFET with charge trap were simulated using Synopsys Sentaurus$^{TM}$. The Shockley-Read-Hall (SRH) and dynamic nonlocal BTBT model were used for accurate characterization. The dynamic nonlocal BTBT model is essential, as it can dynamically determine and calculate all tunneling paths based on the energy band profile. In detail, the BTBT model was calibrated with experimental results, as shown in Fig. 2(a). To calculate the BTBT generation rate ($G$) per unit volume at the uniform electric field limit, Kane's model was used [Eq. (1)] [28].

$$G = A\left(\frac{F}{F_0}\right)^P \exp\left(-\frac{B}{F}\right) \tag{1}$$

The prefactor ($A$) and the exponential factor ($B$) are Kane parameters, while F represents the electric field. For accurate simulation, we calibrated the model parameters by extracting current from the fabricated planar TFET. The calibrated parameters are as follows: $F_0$ = 1 V/m, $P$ = 2.5 for an indirect BTBT, $A_{Si} = 4.0 \times 10^{14}$ cm$^{-3}\cdot$s$^{-1}$, and $B_{Si} = 9.9 \times 10^6$ V/cm are the Kane parameters of Si, and $F$ denotes the electric field. The program rate in the ONO dielectric was also calibrated based on a fabricated Metal-$SiO_2$-$Si_3N_4$-$SiO_2$ capacitor. In the inset of Fig. 2(b), the simple fabrication processes are shown. Each thickness of the dielectric is the same as in the proposed device. The flat band shifts ($\Delta V_{FB}$) were extracted with various program times. The electron tunnel mass was calibrated with the ONO capacitors' electron trapping rate, as shown in Fig. 2(b). To calibrate the electron trapping rate, the electron tunnel mass was fitted with $\Delta V_{FB}$.

## III. SIMULATION RESULTS

Fig. 2(c) represents the energy band at 0.5 V of drain voltage ($V_{DS}$) when cut into the ONO line. When




| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Fig. 4.** (a) Program sequence for achieving the target $V_t$; (b) Program hole density based on the gate pulse; (c) NOR and NAND gates with mixed usage of MOSFETs for reduced resistance circuits; (d) Truth table of logic gate.

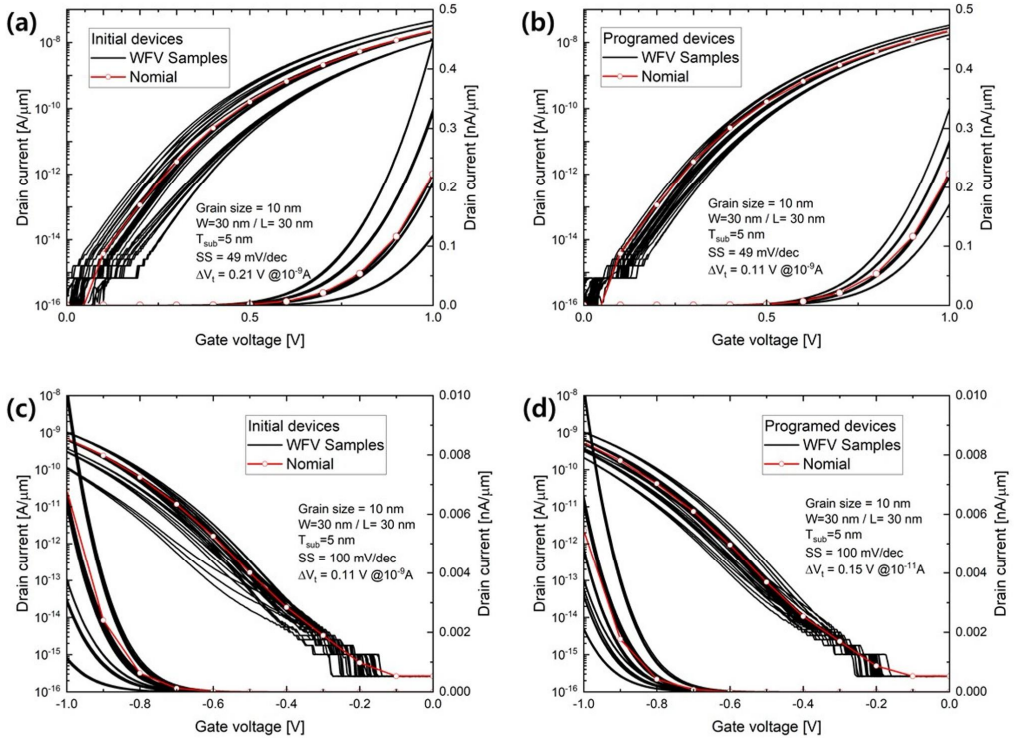



**Fig. 5.** n-type: (a) initial; (b) programmed, p-type; (c) initial; (d) programmed TFET.

program bias is applied in gate, the electrons on drain are moved to the channel and when gate voltage is applied, the electrons are trapped to the nitride region. When programmed, it is found that the energy band in the nitride region has risen by about 4 eV from initial state. And the energy band in the programmed nitride region raises the energy band of the source. Fig. 2(d) shows the transfer characteristics of the charge trap TFET with

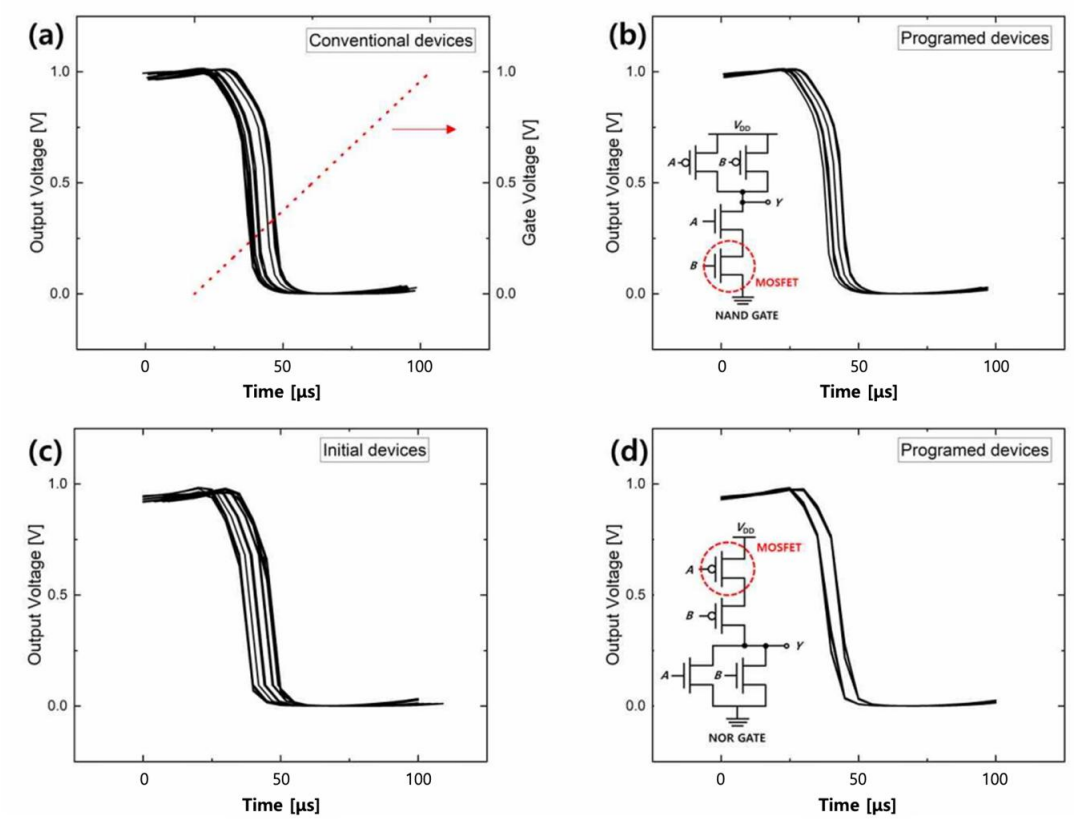



**Fig. 6**. NAND/NOR gate transient simulation: (a) conventional NAND; (b) proposed NAND; (c) conventional NOR; (d) proposed NOR.

various $V_{DS}$. There is no drain induced current enhancement. depending on the $V_{DS}$, so the short channel effect (SHE) can be excluded. And the minimum *SS* is 28.59 mV/dec of $V_{DS}$ = 0.1 V, 29.01 mV/dec of $V_{DS}$ = 0.5 V and 34.62 mV/dec of $V_{DS}$ = 1.0 V. Thus, we found that the *SS* values for $V_{DS}$ changes are below 60 mV/dec. The proposed device is a low power device that can operate at a low gate bias. We confirmed the BTBT generation of the device. Since the proposed device is made of dopingless, as seen in inset of Fig. 2(d), the BTBT region is formed at edge of gate region. Fig. 3(a) shows a BTBT rate of the charge trap TFET from 2 nm to 15 nm of substrate thickness ($T_{sub}$). The proposed device does not form a tunnel barrier through doping, but rather the tunnel barrier region changes with voltage [Fig. 3(b) and (c)]. In other words, electrons are programmed into the charge trap region to form a tunnel barrier, but the depletion region near the Si channel changes due to the operating voltage, causing variations in BTBT occurrence rates. Due to these characteristics, the downside is that high current is not exhibited. However, even if the substrate thickness varies with the process, the current characteristics are determined by voltage, resulting in minimal current variation. Consequently, it has the advantage of high reliability and can be used to create devices that are insensitive to PVT variations.

In Fig. 4(a), a sequential hole program is executed by applying a pulse with a gate voltage of -8 V. After performing a 1-step program, the current is examined at $V_{GS}$ = 0.5 V. If the current value is lower than the target threshold voltage ($V_t$, @ $10^{-12}$ A/μm) additional programming is carried out [Fig. 4(b)]. The configuration of the mixed-signal circuit is depicted in Fig. 4(c). For the NOR/NAND pass gate section, the circuit is constructed using high-performance MOSFETs with good $I_{ON}$ characteristics, while the stack section is implemented with the proposed TFETs. The reason for evaluating a mix of MOSFETs and TFETs in Fig. 4(c) is that using two-stage TFETs would result in excessive degradation due to low current drive and WFV. If the entire circuit were constructed using TFETs, the reduced current drivability of TFETs would result in higher

resistance, leading to a decrease in the output voltage margin. However, since the TFET's characteristic changes due to WFV were fully reflected, as shown in the simulation, a precise evaluation was conducted. Thus, the effect of reducing variation with the proposed device's program has been thoroughly demonstrated. In the NOR/NAND section, out of the two devices connected in series, one is constructed using TFETs. This configuration, due to the low $I_{OFF}$ characteristics of TFETs, results in a truth table based on input, as shown in Fig. 4(d). The output values are inverted based on each input, and the corresponding improvement in voltage variation is measured.

In Fig. 5, the n-type and p-type characteristics of the proposed device are illustrated. For cases Fig. 5(a) and (c), the program time and voltage were fixed at 8 V and 0.01 sec, respectively, to depict the scatter of the transfer curve concerning WFV. In cases Fig. 5(b) and (d), results are shown where the program pulse was adjusted using the bias scheme from Fig. 4(a) to reduce the $V_t$ variation. In the case of n-type, it exhibited a 0.1 V decrease in $V_t$ variation, while for p-type, there was a 0.04 V reduction in variation.

In Fig. 6, the operation of the proposed device's NAND gate is depicted based on the presence or absence of programming. The bottom-most device was constructed using MOSFETs to reduce resistance, while the rest of the devices were formed using the proposed TFETs. The variation in transition time due to $V_t$ differences was observed. Specifically, it can be observed that before programming, $\Delta t$ (time variation) reduced from 10.7 μs to 6.3 μs [Fig. 6(a) and (b)]. A similar reduction was also observed in NOR, decreasing from 11.1 μs to 6.2 μs [Fig. 6(c) and (d)]. This ultimately translates to a minimum 41 % improvement in the operating frequency margin.

## IV. Conclusion

In conclusion, this study has provided valuable insights into the electrical characteristics of dopingless TFETs featuring ONO gate insulator stacks. The research has demonstrated the potential benefits of employing ONO structures to reduce the impact of WFV on the channel, paving the way for more reliable TFET-based devices. The study's exploration of TFETs' immunity to WFV and current variations compared to doping-based junctions has important implications for future device design and optimization. These findings have the potential to enhance the performance and reliability of TFETs in various applications, particularly in low-power applications. In other words, the proposed device's current can be precisely tuned, allowing for consistent current output despite changes in process, voltage, and temperature. This characteristic makes it highly applicable in logic circuits that require stable characteristics, such as bandgap generators and temperature sensors [29-31]. Overall, the findings of this study hold promise for the development of more robust and efficient TFET-based devices, and the insights gained may lead to advancements in semiconductor technology, ultimately benefiting a wide range of industries and applications.

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