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A Second-order Delta-sigma Modulator for Battery Management System DC Measurement

Ji-Ho Park, Jun-Ho Boo, Jae-Geun Lim, Hyoung-Jung Kim, Jae-Hyuk Lee, Seong-Bo Park, Joo-Yeul Yang, and Gil-Cho Ahn

***Abstract*:** This paper presents a second-order modified feed-forward (FF) delta-sigma modulator for battery management system DC measurement. The proposed ADC employs a modified 3-bit feedback digital-to-analog converter (DAC) with the data weight averaging (DWA) technique to improve the capacitance matching. The modified 3-bit DAC reduces the logic complexity of the DWA by simplifying the switching network of unit capacitors. Additionally, the proposed ADC adopts capacitor swapping technique between the input and reference sampling capacitors to minimize its gain error. To further improve the performance of the proposed ADC, system-level low-frequency chopping (CHL) and correlated double sampling (CDS) are employed to mitigate offset and flicker noise. The prototype ADC is fabricated in a 180 nm CMOS process, and the core area is 0.53 mm^2. It consumes 9.48 μW from a 1.8 V supply voltage at an operating clock frequency of 19.2 kHz with an oversampling ratio (OSR) of 256. It achieves a dynamic range (DR) of 102.4 dB, a resolution of 7 μV_{rms}, and an offset of 6.86 μV, resulting in a Schreier figure-of-merit (FoM) of 165.3 dB.

***Index terms*:** Analog-to-digital converter (ADC), delta-sigma modulator, data weight averaging (DWA), digital-to-analog converter (DAC), feed-forward (FF)

I. INTRODUCTION

In a battery management system (BMS), a voltage sensing integrated circuit (IC) is an essential block for monitoring the state of charge (SOC), which indicates the remaining power of the battery cells [1-4]. Fig. 1 illustrates the block diagram of the voltage sensing IC for BMS, which consists of a high voltage multiplexer (HVMUX) to select battery cells, a level shifter to scale down the high voltage of the battery cells, a voltage reference generator, and an analog-to-digital converter (ADC) [1]. Among these, the key building block is the ADC which requires high-resolution, and delta-sigma ADCs are well suited for the voltage sensing because they can achieve high accuracy through oversampling and noise shaping [5,6].

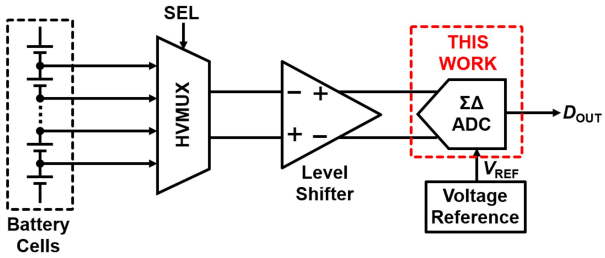

Fig. 1. Block diagram of the voltage sensing IC for BMS.

In the delta-sigma ADCs, an input feed-forward (FF) topology is widely used for high-resolution because it eases the design requirements of the integrators by processing the quantization noise only [7]. This allows for the reduction of quantization noise and the swing range of the integrators by employing a multi-bit digital-to-analog converter (DAC), and the DWA is used to correct the mis-

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Department of Electronic Engineering, Sogang University, Seoul 04107, Korea
E-mail : gcahn@sogang.ac.kr

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match of unit capacitors in the DAC [8]. However, due to signal attenuation within the internal FF path, the comparator accuracy requirements become more challenging, and the load capacitance of the first integrator is affected by the quantizer, reducing power efficiency. Given these constraints, the modified FF topology [9,10], which removes the internal FF path, has emerged. The load capacitance of the first integrator is no longer affected by the quantizer, and simplified passive summing reduces signal attenuation.

In addition to the power efficient topology described above, the proposed architecture employs a modified 3-bit feedback DAC with data weight averaging (DWA). The modified DAC reduces the complexity of the DWA logic, thereby increasing power and area efficeincy. The proposed modulator is fabricated in a 180 nm CMOS process, and achieves a dynamic range (DR) of 102.4 dB and a Schreier figure-of-merit (FoM) of 165.3 dB.

The rest of this article is organized as follows: Section II explains the architecture of the proposed delta-sigma modulator. Section III discusses the details of the circuit implementation. The measurement results of the prototype modulator are presented in Section IV, and this article concludes with Section V.

II. Proposed Architecture

The architecture of the proposed delta-sigma modulator is shown in Fig. 2. The modulator employs the modified FF topology and consists of a first integrator, a second integrator with an analog signal processing block, $H_A(z)$, a 3-bit flash quantizer with a passive switched capacitor (SC) adder, and a feedback DAC with DWA. The output of the modulator, $D_O(z)$, and the outputs of two integrators, $V_1(z)$ and $V_2(z)$, are given by

$$D_O(z) = U(z)\cdot STF(z) + Q(z)\cdot NTF(z), \tag{1}$$

$$V_1(z) = Q(z)\cdot z^{-\frac{1}{2}}\cdot(1-z^{-1}), \tag{2}$$

$$V_2(z) = Q(z)\cdot z^{-1}\cdot(2-z^{-1}), \tag{3}$$

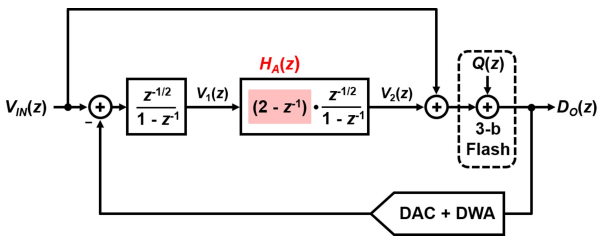


Fig. 2. Architecture of the proposed delta-sigma modulator.

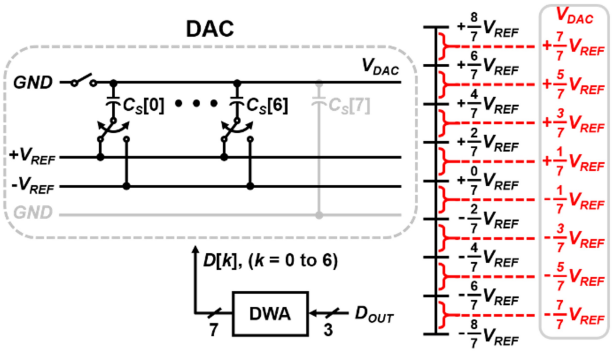


Fig. 3. The modified DAC with DWA and the output levels.

where $V_{IN}(z)$ and $Q(z)$ indicate the input of the modulator and quantization noise, respectively. Thanks to the modified FF topology, integrators handle only quantization noise as shown in (2) and (3), which reduces the swing range of the integrators [9,10]. Also, due to $H_A(z)$ in the modified FF architecture, the design requirement of the comparators is relaxed, and power efficiency is increased.

For the feedback DAC, the proposed ADC adopts a modified 3-bit DAC with seven unit capacitors, removing one capacitor connected to ground, as shown in Fig. 3. In the modified DAC, all of the bottom plates of the capacitors switch only between $+V_{REF}$ and $-V_{REF}$, which simplifies the DWA logic complexity. The DAC output ranges from $-7/7V_{REF}$ to $+7/7V_{REF}$ in steps of $2/7V_{REF}$. To reduce the mismatch between unit capacitors, the conventional DWA technique is applied [8].

III. Circuit Implementation

1. Proposed Delta-Sigma Modulator

The overall schematic of the proposed delta-sigma modulator and its timing are shown in Fig. 4. The modulator is implemented in a fully differential structure and operates with two non-overlapping clocks, ϕ_1 and ϕ_2. In the first integrator, DWA is employed to minimize the capacitance mismatch, and its operation is as follows. In the ϕ_1 phase, the flash quantizer determines the 3-bit digital output, and in the ϕ_2 phase, the reference sampling capacitors are shifted according to the output code. Two additional clock signals ϕ_3 and ϕ_4 are employed to implement the transfer function $2-z^{-1}$of the second integrator.

Using the thermal noise analysis presented in [11], the sampling capacitance values for both integrators were determined. To reduce the degradation of modulator performance due to thermal noise, the total sampling capaci-

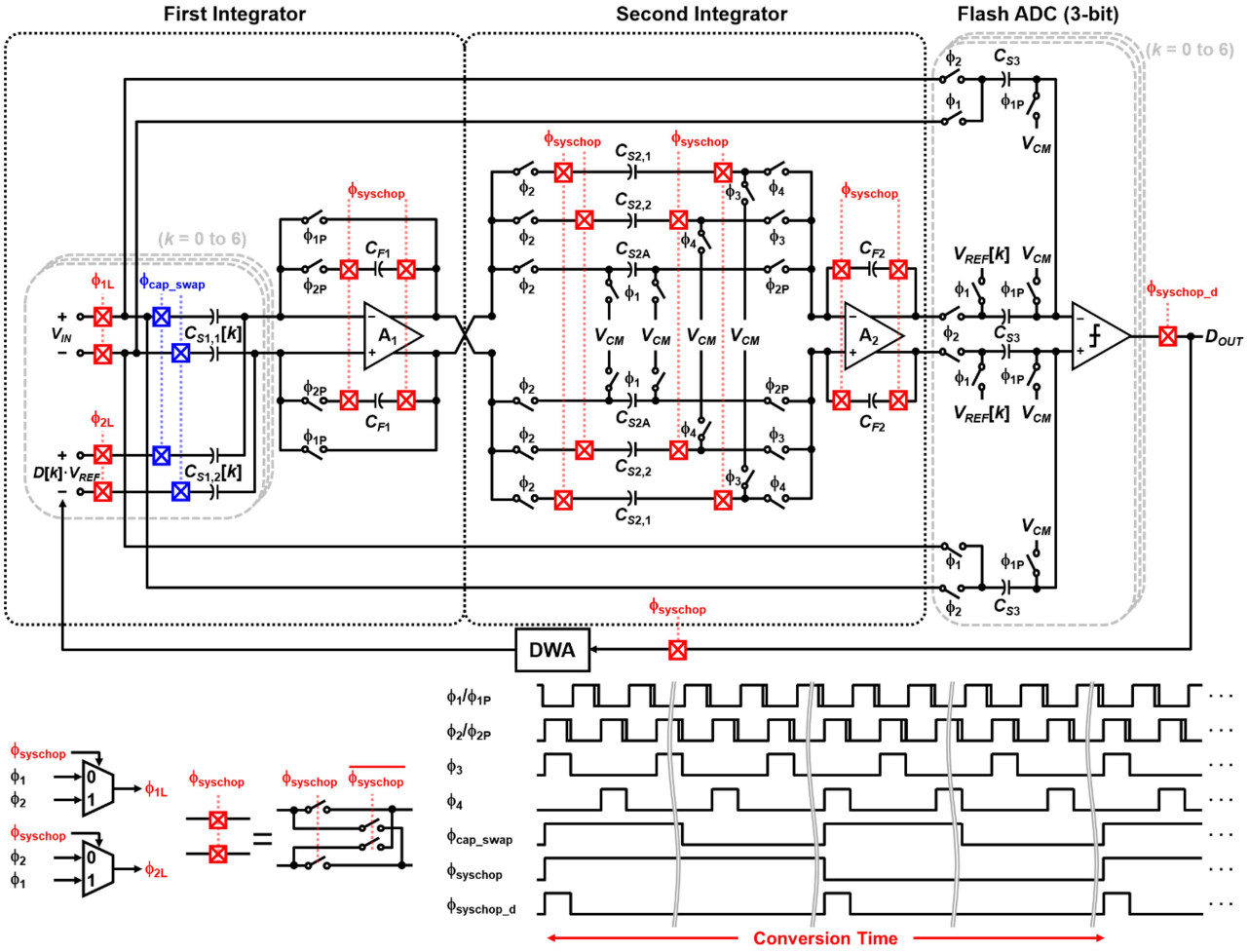


Fig. 4. The overall schematic of the proposed second-order modified FF delta-sigma modulator and its timing.

tance of the first integrator is set to be 1.5 pF, that of the second integrator to 200 fF, and the input capacitance of the quantizer to 100 fF, since the thermal noise generated in the second integrator and the quantizer is shaped, allowing for smaller capacitor values [11].

A resistive-ladder (R-ladder) has been used on-chip to generate the reference voltage for the flash quantizer. Since static current is produced in the R-ladder, increasing the total resistance reduces power consumption. However, feedthrough caused by the input stage capacitance between the quantizer's input and the reference voltage leads to distortion in the ADC [12]. To address this, the maximum feedthrough at the midpoint of the R-ladder is limited to 0.1 LSB. The total resistance is determined by the following equation

$$R = \frac{4\phi}{\pi 2^n f_{in} C}, \tag{4}$$

where ϕ is the feedthrough in LSB and n is the resolution of the quantizer and C is the total capacitance from the R-ladder, and f_{in} is the input frequency of the quantizer [12]. As a result, the total resistance must be set below 1.18 MΩ. Considering feedthrough and static current, a total resistance of 0.93 MΩ was chosen. This R-ladder occupies an area of 0.07 mm^2.

Correlated double sampling (CDS) is employed in the first integrator to mitigate offset and flicker noise [13]. Furthermore, A system-level low-frequency chopping (CHL) technique suppresses the residual offset of the modulator by periodically inverting the polarity of the input and output [14]. Therefore, chopped switches are employed at the input and output paths. In this design, the chopped switch control clock, $\phi_{syschop}$, is used to enable one CHL transition in one conversion cycle. To match the polarity of the integration path between before and after the CHL transition, chopped switches are employed for the feedback capacitors. Additionally, the chopped switches are also employed in the sampling ca-

pacitors of the second integrator, except for the additional sampling capacitor, C_{S2A}, which is reset in the ϕ_1 phase.

During the first reference sampling after the CHL transition, since the modulator output which provides feedback to the DAC has the same polarity as the previous state, a $\phi_{syschop\_d}$ clock signal is used to invert the output polarity of the feedback path to match the polarity of the input and feedback DAC [15]. This process modulates the systematic offset and removes it after passing through the decimation filter.

2. Loop Filter

The schematic of the first integrator and its timing are shown in Fig. 5. Bootstrapped switches are employed to enhance input sampling linearity [16]. To reduce ADC gain error caused by the capacitance mismatch between the input sampling capacitor $C_{S1,1}[k]$ and the reference sampling capacitor $C_{S1,2}[k]$, a capacitor swapping technique is employed to average out the capacitance mismatch as follows: During one conversion cycle, the $C_{S1,1}[k]$ and $C_{S1,2}[k]$ arrays are swapped twice to ensure that the averaged capacitance is used for both input and reference sampling. The schematic of the second integrator with the transfer function, $2-z^{-1}$, and its timing are shown in Fig. 6. For the second integrator, three sampling capacitors are employed: two sampling capacitors $C_{S2,1}$, $C_{S2,2}$, and an additional capacitor C_{S2A}. During the following ϕ_3 phase, $C_{S2,2}$ and C_{S2A} are connected to integrate the output of the first integrator $V_1[n-1]$ without delay. At this time, the remaining $C_{S2,1}$ samples the output of the first integrator. Then, during the subsequent ϕ_1 phase, C_{S2A} is reset. In the following ϕ_4 phase, similar to the ϕ_3 phase, the previously sampled $C_{S2,1}$ and C_{S2A} are connected for integration. Finally, the output of the second integrator $V_2[n]$ becomes $2\cdot V_1[n]-V_1[n-1]$, and this sequence of operations implements the transfer function $2-z^{-1}$.

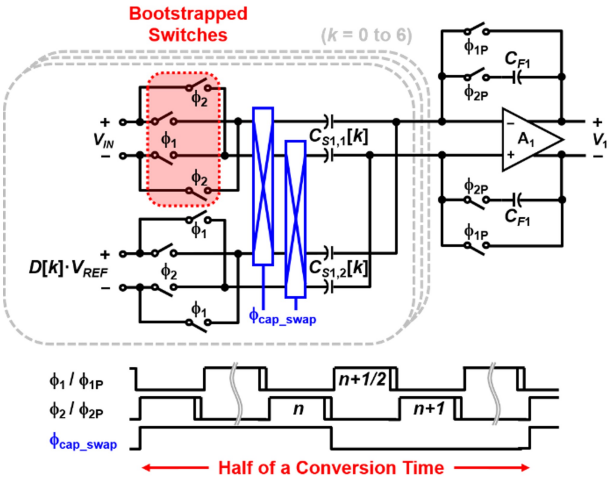


Fig. 5. Schematic of the first integrator and its timing.

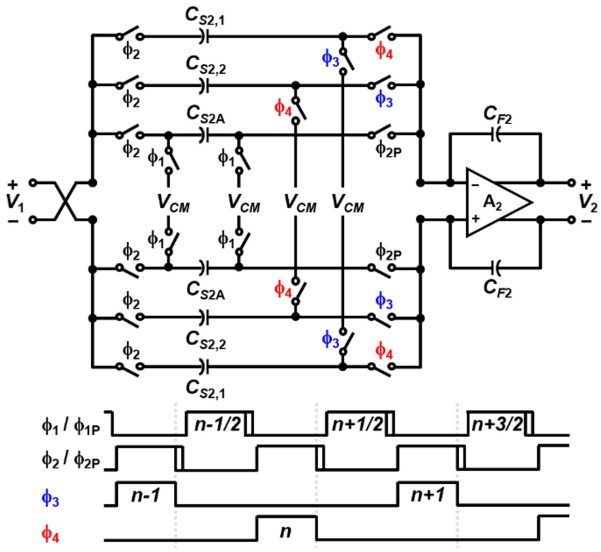


Fig. 6. Schematic of the second integrator and its timing.

IV. Measurement Results

The prototype delta-sigma modulator is implemented in a 180 nm CMOS process. Fig. 7 shows the die micrograph of the proposed modulator. The core area is 0.53 mm^2. Fig. 8 shows the power breakdown of the proposed modulator. From a 1.8 V supply, the modulator consumes 9.48 μW at 19.2 kHz sampling frequency. Fig. 9 shows the measured output spectrum of the proposed modulator with a 0.6 V DC input and input shorted, respectively. The measured DR is 102.4 dB and Fig. 10 shows the measured offset

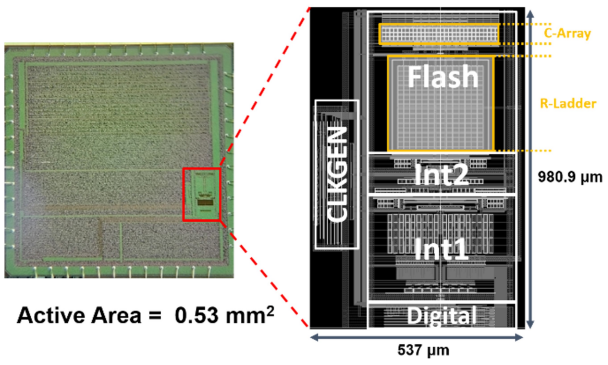


Fig. 7. Die micrograph of the proposed modulator.

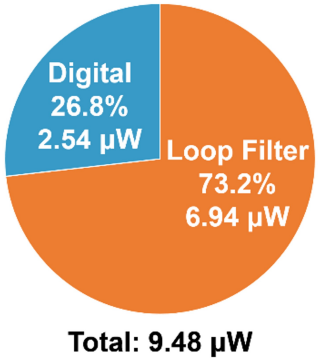


Fig. 8. Power breakdown of the proposed modulator.

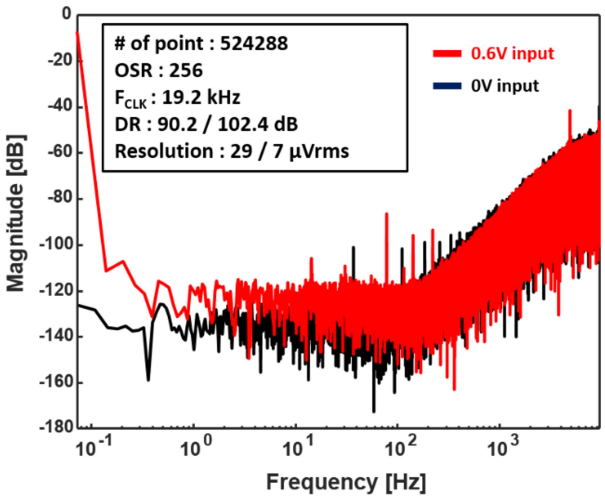
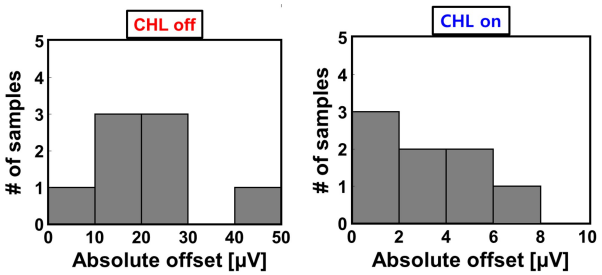


Fig. 9. Measured output spectrum of the proposed modulator.



(a) (b)

Fig. 10. Measured offset of the proposed modulator with (a) chopped off, and (b) chopped on.

with and without CHL, and for this measurement, a sinc^3 filter is implemented off-chip for decimation in MATLAB. The maximum offset from eight samples without CHL is 50 μV, and it drops below 6.86 μV with CHL. The measured performance of the proposed modulator is summarized and compared in Table 1.

Table 1. Performance summary and comparison table.

	This work	[17]	[18]	[19]	[20]
Architecture	DT DSM	CT DSM	CT DSM	DT IDSM	DT DSM
Process (nm)	180	65	180	180	110
F_{CLS} (kHz)	19.2	0.512	64	5000	512
OSR	256	256	128	250	128
BW (Hz)	18.75	1	250	10000	2000
Supply (V)	1.8	1.2	1.8	1.8	1.5
Power (μW)	9.48	15	2.16	83	62.43
DR (dB)	102.4	105	81.4	89.1	96.3
Resolution (μV_{rms})	7	4	-	19	-
Offset (μV)	6.86	-	-	-	-
Area (mm^2)	0.523	9.07	0.29	0.35	0.165
*FoM$_s$	165	153	162	162	171

*FoM$_s$ = DR +10 $\cdot$ log$_{10}$(BW/Power)

V. Conclusion

This paper presents a second-order modified FF delta-sigma modulator for BMS DC measurement. The proposed modulator employs the modified 3-bit feedback DAC to reduce the complexity of the DWA logic, and a capacitor swapping technique is adopted to minimize the gain error from sampling capacitance mismatch. Additionally, the CDS and CHL techniques are applied to minimize offset and flicker noise. The prototype modulator, fabricated in a 180 nm CMOS process, achieved a DR of 102.4 dB, a resolution of 7 μV_{rms}, and an offset of 6.86 μV while consuming 9.48 μW.

Acknowledgments

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Ji-Ho Park received the B.S. degree in electronic engineering from Sogang University, Seoul, Korea, in 2023, where he is currently pursuing the M.S. degree. Mr. Park is a recipient of a scholarship sponsored by Samsung electronics. His current research interests include high-resolution data converters and sensor interfaces.

Jun-Ho Boo received the B.S. and Ph.D. degrees in electronic engineering from Sogang University, Seoul, Korea, in 2017 and 2023, respectively. From 2023 to 2025, he was a Staff Engineer at Memory Division, Samsung Electronics, Hwaseong, Korea. His current research interests include analog and mixed-signal circuits, data converters, and sensor interfaces.

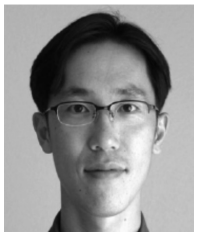
Jae-Geun Lim received the B.S. degree in electronic engineering from Sogang University, Seoul, Korea, in 2019, where he is currently pursuing the Ph.D. degree. Mr. Lim is a recipient of a scholarship sponsored by Samsung electronics. His current research interests include low-power and high-speed analog-to-digital converter.

Hyoung-Jung Kim received the B.S. degree in electronic engineering from Sogang University, Seoul, Korea, in 2020, where he is currently pursuing the Ph.D. degree. Mr. Kim is a recipient of a scholarship sponsored by Samsung electronics. His current interests are in the design of low-power and high-speed analog-to-digital converter.

Jae-Hyuk Lee received the B.S. degree in electronic engineering from Sogang University, Seoul, Korea, in 2020, where he is currently pursuing the Ph.D. degree. Mr. Lee is a recipient of a scholarship sponsored by Samsung electronics. His current interests are in the design of high-speed, high-resolution CMOS data converters, and very high-speed mixed-mode integrated systems.

Seong-Bo Park received the B.S. degree in electronic engineering from Sogang University, Seoul, Korea, in 2022, where he is currently pursuing the Ph.D. degree. His current research interests include data converters, and sensor interfaces.

Joo-Yeul Yang received the B.S. degree in electronic engineering from Sogang University, Seoul, Korea, in 2023, where he is currently pursuing the M.S. degree. Mr. Yang is a recipient of a scholarship sponsored by Samsung electronics. His current research interests include data converters and mixed-signal circuit design.



Gil-Cho Ahn received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, in 1994 and 1996, respectively, and the Ph.D. degree in electrical engineering from Oregon State University, Corvallis, in 2005. From 1996 to 2001, he was a Design Engineer at Samsung Electronics, Kiheung, Korea, working on mixed analog-digital integrated circuits. From 2005 to 2008, he was with Broadcom Corporation, Irvine, CA, working on AFE for digital TV. Currently, he is a Professor in the Department of Electronic Engineering, Sogang University. His research interests include high-speed, high-resolution data converters and low-voltage, low-power mixed-signal circuits design.