JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL. 25, NO. 1, FEBRUARY, 2025
https://doi.org/10.5573/JSTS.2025.25.1.66
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A Compact Wide-swing Self-biased Cascode Current Mirror for Wide Dynamic-range Applications

Seongil Yeo, Jaejin Kim, Gunmo Koo, and Kunhee Cho

***Abstract*:** The cascode current mirror is the most widely used block in analog circuit design, and wide voltage swing operation is essential for low-supply voltage applications. In wide dynamic-range applications, such as current sensing in DC-DC converters, the current mirror must maintain high accuracy across a wide range of reference currents while enabling wide voltage swing operation at the maximum reference current. In this paper, a wide-swing self-biased cascode current mirror for wide dynamic-range applications is described. Unlike conventional structures, the proposed design is biased by a non-isolated active device without using an extra current path or an isolated active device. The proposed current mirror demonstrates higher accuracy for a wide-range of reference currents compared to prior wide-swing cascode current mirror designs and offers a more compact design.

***Index terms*:** Cascode current mirror, low-voltage, self-biased, wide-swing, wide dynamic-range

I. INTRODUCTION

The current mirror is a fundamental design block in analog integrated circuits, providing both supply and reference currents to each design block. The cascode current mirror is widely used due to its larger output resistance and greater mirroring accuracy compared to the single-ended current mirror [1]. To reduce the voltage headroom in low-supply voltage, wide voltage swing operation is required for the cascode current mirror [2]. Moreover, wide dynamic-range operation is crucial for applications where the reference current varies over a wide range [3]. For instance, current sensing in switching power converters [4,5] necessitates a wide dynamic-range current mirror. Fig. 1 shows the high-side (HS) and low-side (LS) current sensing circuits in a switching power converter. The current sensing circuit is followed by the current mirror to utilize the sensed current information. Since the inductor current can be varied by the output load (R_L), inductance (L), switching frequency, and duty-cycle, the following current mirror has to operate at a wide dynamic-range. In particular, when the switching power converter operates in the discontinuous conduction mode (DCM), the inductor current may drop to 0 A. Therefore, the current mirror has to be designed to cover the current levels ranging from 0 A to the maximum current rating of the inductor.

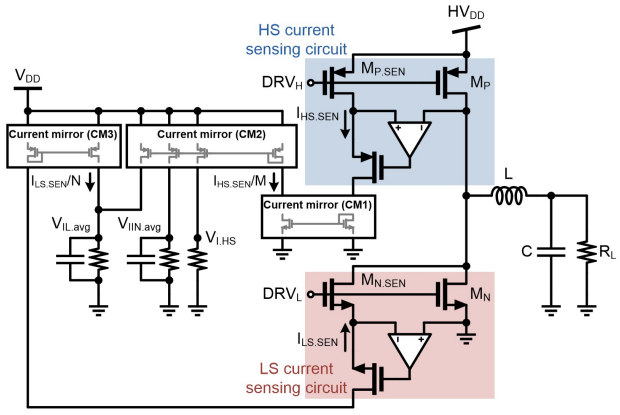


Fig. 1. High-side and low-side current sensing circuits in the switching power converter.

In this paper, a wide-swing self-biased cascode current mirror designed for wide dynamic-range applications is described. Unlike conventional cascode current mirrors,

Manuscript received Apr. 20, 2024; revised May 31, 2024; accepted Jun. 27, 2024
School of Electronics Engineering, Kyungpook National University, Daegu, Korea
Department of Semiconductor Convergence Engineering, Sungkyunkwan University, Suwon, Korea
E-mail : kunhee@knu.ac.kr, kunhee@skku.edu

the proposed structure is compact and demonstrates high accuracy across a wide dynamic-range while maintaining a wide voltage swing at the output.

This paper is organized as follows. Section II introduces the conventional cascode current mirrors. Section III describes the proposed wide-swing cascode current mirror and Section IV provides the circuit implementation and measurement results, followed by the conclusion in Section V.

II. Conventional Cascode Current Mirrors

Fig. 2 shows the different types of conventional wide-swing cascode current mirrors. The cascode current mirror consists of four transistors M_{N1}, M_{N2}, M_{N3}, and M_{N4}. A wide voltage swing can be achieved by connecting the gate of M_{N1} and M_{N2} (V_{G1}) to the drain of M_{N3}, and properly biasing the gate of M_{N3} and M_{N4} (V_{G2}). Assuming that the same sized NMOS transistors are used for M_{N1}, M_{N2}, M_{N3}, and M_{N4} in implementing the cascode current mirror and ignoring the body effect, V_{G2} should be biased as follows [6]:

$$V_{G2} = V_T + 2V_{OV}, \tag{1}$$

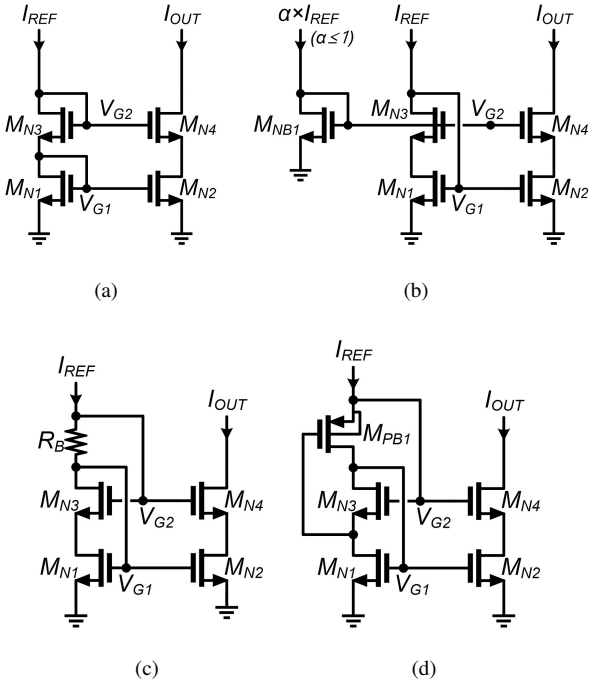


Fig. 2. Cascode current mirrors. (a) Baseline structure. (b) Biased by the extra current path. (c) Self-biased by the resistor. (d) Self-biased by the isolated active-device [6].

where V_T and V_{OV} are the threshold and overdrive voltage of the NMOS used in the current mirror, respectively.

The V_{G2} can be biased with an extra current path as shown in Fig. 2(b). In addition to the reference current path, the extra current path is added and bias the V_{G2} to $V_T + 2V_{OV}$ by setting the overdrive voltage of M_{NB1} to $2V_{OV}$. Although, this structure can achieve wide-swing and wide dynamic-range operation, it is not preferable to use in the current mirrors of CM1 and CM3 in Fig. 1, because the extra current path requires an additional current sensing circuit. Therefore, the self-biased current mirror structure is necessary here.

The wide-swing self-biased cascode structure can be implemented using a resistor (R_B) or an isolated-active device (M_{PB1}) [7] as shown in Figs. 2(c) and 2(d), respectively. The V_{G2} can be self-biased by choosing the R_B value to set the voltage drop across the R_B to V_{OV} [Fig. 2(c)]. However, self-biasing with a resistor is not suitable for the wide dynamic-range applications because the voltage drop across the resistor is proportional to the reference current (I_{REF}), while V_{OV} is proportional to the $\sqrt{I_{REF}}$. To resolve this issue, the isolated-active device (M_{PB1}) can be used as shown in Fig. 2 (d) [7]. Assuming the threshold voltage of PMOS and NMOS are nearly identical, V_{G2} can be set to $V_T + 2V_{OV}$ by setting the V_{OV} of M_{PB1} to the same value as the V_{OV} of M_{N3}. Therefore, the ΔV_{G2} is proportional to $\sqrt{I_{REF}}$ allowing V_{G2} to track $V_T + 2V_{OV}$ across a wide range of the reference currents. However, this approach requires the isolated MOSFET to use as an active-device, which increases the die size. In addition, it cannot be used for P-type current mirror if the deep N-well process is not supported which is essential for using an isolated NMOS transistor.

III. Proposed Wide-swing Cascode Current Mirror

Fig. 3 shows the proposed wide-swing self-biased cascode current mirror, which employs the non-isolated active-device. A P-type active-device is used for the NMOS current mirror [Fig. 3(a)], with its gate connected to *GND*, and an N-type active-device is used for the PMOS current mirror [Fig. 3(b)], with its gate connected to the supply-voltage (V_{DD}). In the proposed structure, V_{G2} is determined by the V_{SG} of M_{PB2}, however, the body effect has to be considered since a non-isolated active-device is used. Therefore, V_{G2} in Fig. 3(a) can be expressed as fol-

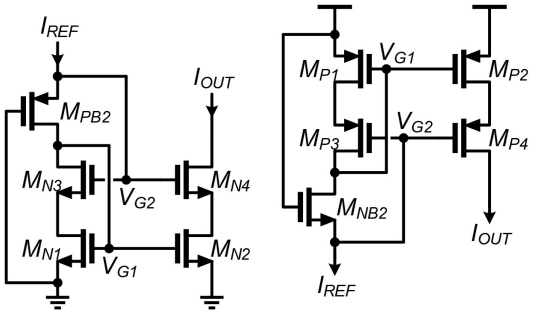
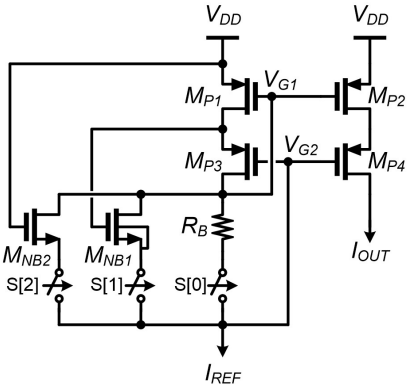


Fig. 3. Proposed wide-swing self-biased cascode current mirrors. (a) NMOS current mirror self-biased by the P-type active-device. (b) PMOS current mirror self-biased by the N-type active-device.



(a)

M_{P1}~M_{P4}	M_{NB1}	M_{NB2}	R_B
$L = 0.5\ \mu$m $W = 2\ \mu$m	$L = 3\ \mu$m $W = 6\ \mu$m	$L = 3\ \mu$m $W = 5\ \mu$m	25 kΩ

(b)

Fig. 4. (a) Schematic of implemented self-biased wide-swing current mirror. (b) Circuit parameters.

lows:

$$V_{G2} = V_{T0,PB2} + \Delta V_{T,PB2} + V_{OV,PB2}, \tag{2}$$

where V_{T0} is the threshold voltage without the body effect, ΔV_{T2} is the amount of threshold voltage varies caused by the body effect. $\Delta V_{T,PB2}$ also can be expressed as follows:

$$\Delta V_{T,PB2} = \gamma\left(\sqrt{|-2\phi_F + V_{SB,PB2}|} - \sqrt{|2\phi_F|}\right), \tag{3}$$

where γ, ϕ_F, and V_{SB} are the body effect coefficient, the fermi potential of the substrate, and the body-to-source voltage, respectively. Since the $|V_{SB,PB2}|$ is increased by $\sqrt{I_{REF}}$, $\Delta V_{T,PB2}$ is inverse proportional to $\sqrt[4]{I_{REF}}$. Therefore, ΔV_{G2} is proportional to $\sqrt{I_{REF}}$ by $V_{OV,PB2}$ term and inverse proportional to $\sqrt[4]{I_{REF}}$ by the body effect.

When considering a wide-range of I_{REF}, the body effect becomes less effective at high I_{REF}, and V_{G2} can be approximated as $V_{T0,PB2} + V_{OV,PB2}$. Assuming that the threshold voltage of PMOS and NMOS are nearly the same, $V_{OV,PB2}$ is set to $V_{OV,N1} + V_{OV,N2}$ by appropriately sizing M_{PB2} to achieve wide-swing operation. On the other hand, at low I_{REF}, $V_{OV,PB2}$ is almost negligible, and V_{G2} can be approximately as $V_{T0,PB2} + \Delta V_{T,PB2}$, whereas V_{G2} is $V_{T0,PB1}$ in the conventional approaches [Figs. 2(b) and 2(d)]. Thus, the proposed approach shows a higher V_{G2} due to the body effect of the biasing device (M_{PB2}), which is beneficial in reducing current mirror mismatch at low I_{REF}. In conventional current mirrors, the V_{DS} of M_{N1} and M_{N2} decreases to a small value at low I_{REF}, and even a small mismatch of V_{DS} between M_{N1} and M_{N2} can lead to significant current mirror mismatch. By applying a higher V_{DS} of M_{N1} and M_{N2} in the proposed approach, the channel length modulation can be suppressed, and current mirror mismatch can be reduced. Therefore, a wider range of I_{REF} with lower current mirror mismatch can be achieved in the proposed structure. The design procedure is very simple, requiring the sizing of M_{PB2} to satisfy Eq. (2) to meet Eq. (1) at the highest I_{REF}. This ensures that the current mirror maintains high accuracy over a wide-range of I_{REF}.

IV. Circuit Implementation and Measurement Results

The proposed wide-swing self-biased current mirror has been implemented in 0.18 μm CMOS process. Fig. 4 shows the schematic of the implemented self-biased current mirror along with its parameters. To ensure a fair comparison among different bias devices, a single cascode current mirror ($M_{P1} - M_{P4}$) is utilized, and different bias devices can be selected by S[2:0]. As a result, the current mirror can be tested with the proposed bias device (M_{NB2}) as well as conventional bias devices (R_B and M_{NB1}). In addition, by employing the same mirrored circuit ($M_{P1} - M_{P4}$), the performance mismatch caused by process variation can be avoided.

For wide dynamic-range applications, the wide-swing operation has to be achieved at the maximum I_{REF}, ensuring that the voltage swing is not limited through the entire range of I_{REF}. Therefore, the bias devices (R_B, M_{NB1}, and M_{NB2}) are sized appropriately that V_{G2} is set to almost the same level at the maximum I_{REF}, ensuring a consistent

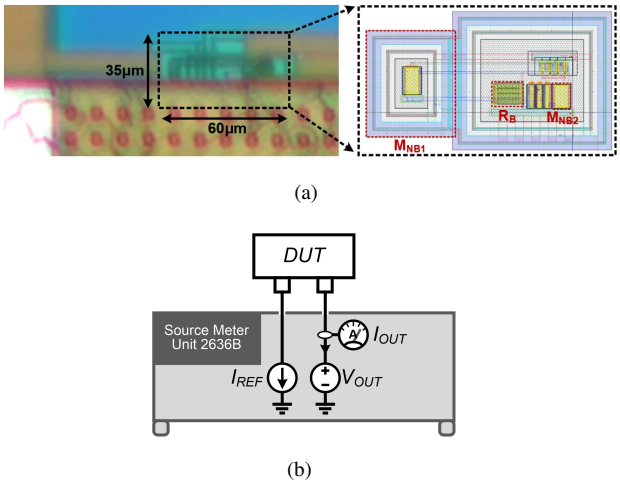


Fig. 5. (a) Chip photograph and layout. (b) Test-setup.

maximum voltage swing performance. Once the highest voltage swing is set at the maximum I_{REF}, the dynamic-range of I_{REF} can be fairly compared by decreasing its level.

Fig. 5 depicts the chip photograph, and layout. The sizes of R_B, M_{NB1}, and M_{NB2} are 40 μm^2, 557 μm^2, and 28 μm^2, respectively. The M_{NB1} occupies a relatively large area due to its requirement for an isolated device, which utilizes a deep N-well process to isolate the body of M_{NB1} from the P-substrate. The supply voltage of 1.8 V is applied, and V_{OUT} is set to 0.5 V. The I_{REF} is varied from 30 nA to 40 μA, and the mismatch of current mirror is shown in Fig. 6. At low I_{REF}, the mismatch of the current mirror biased by the resistor structure is degraded because the voltage drop across the resistor is proportional to the I_{REF}, which is not suitable for the wide dynamic-range operation. The mismatch results for both the biased by the isolated and non-isolated active devices are similar. Fig. 7 shows the measured current mirror mismatch at different temperature with the I_{REF} of 100nA. The current mirror biased by the resistor shows significant mismatch variation compared to the active device biasing methods due to the difference in temperature coefficient between the resistor and the threshold voltage of the transistors.

Table 1 summarizes the performance and provides a comparison with other biasing structure. The proposed structure can achieve $\times$333 wider dynamic-range compared to the resistor based biasing structure. Furthermore, it is a compact design that can achieve wide dynamic-range without the requirement for an isolated active device. The area of the bias device is reduced by approximately 20 times compared to prior work [7], while achieving a similar wide dynamic range.

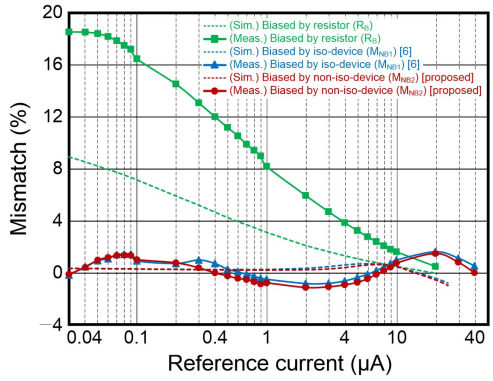


Fig. 6. Measured current mirror mismatch at different I_{REF}.

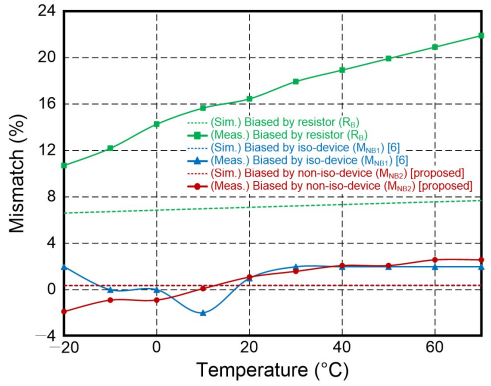


Fig. 7. Measured current mirror mismatch at different temperature with I_{REF} of 100 nA.

Table 1. Performance comparison.

Bias type	Resistor	Isolated active-device [7]	Non-isolated active-device [Proposed]
Dynamic range*	$\times$4 (5 μA-20 μA)	$\times$1333 (30 nA-40 μA)	$\times$1333 (30 nA-40 μA)
Mismatch range	0.5%-18.6%	−0.9%-1.6%	−1.1%-1.5%
Isolated device requirement	No	Yes	No
Bias device size	40 μm^2	557 μm^2	28 μm^2

* Dynamic-range is defined by the I_{REF} range with the mismatch within 3%

V. CONCLUSIONS

A wide-swing self-biased cascode current mirror for wide dynamic-range is demonstrated. The proposed struc-

ture can achieve high accuracy and wide voltage swing over a wide range of I_{REF} without requiring an extra current path or an isolated active device. The implemented current mirror was tested with different bias devices, showing better current mirror mismatch and $\times 333$ wider dynamic-range compared to conventional resistor-based biasing structure. It is also a compact design that can be easily biased by a non-isolated active device.

ACKNOWLEDGMENTS

This work was supported in part by the Institute of Information and Communications Technology Planning and Evaluation (IITP) grant funded by the Korea Government (MSIT) through the Project "Development of High Performance Processing-in-Memory Technology based on DRAM" under Grant 2022-0-01037; and in part by Korea Planning & Evaluation Institute (KEIT) grant funded by the Korea Government (MOTIE) under Grant RS-2024-00404313 (Development of a 650 V GaN-based power converter single IC for mobile device charging adapter). The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] O. Charlon and W. Redman-White, "Ultra high-compliance CMOS current mirrors for low voltage charge pumps and references," *Proc. of IEEE European Solid-State Circuits Conf. (ESSCIRC)*, pp. 227-230, Sep. 2004.

[2] F. Ledesma, R. Garcia, and J. Ramirez-Angulo, "Comparison of new and conventional low voltage current mirrors," *Proc. of Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. II-49-II-52, Aug. 2002.

[3] E. Bruun and P. Shah, "Dynamic range of low-voltage cascode current mirrors," *Proc. of IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. 1328-1331, Apr. 1995.

[4] D. Park and H. Lee, "Improvements in light-load efficiency and operation frequency for low-voltage current-mode integrated boost converters," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 61, no. 8, pp. 599-603, Aug. 2014.

[5] M. Du, H. Lee and J. Liu, "A 5-MHz 91% peak-power-efficiency buck regulator with auto-selectable peak- and valley-current control," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1928-1939, Aug. 2011.

[6] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., McGraw-Hill Education, USA, 2017.

[7] M. Akbari, A. Javid, and O. Hashemipour, "A high input dynamic range, low voltage cascode current mirror and enhanced phase-margin folded cascode amplifier," *Proc. of IEEE Iranian Conf. Elec. Eng. (ICEE)*, pp. 77-81, May 2014.

Seongil Yeo received his B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, Korea, in 2022 and 2024, respectively. He is currently working toward the Ph.D. degree in semiconductor convergence engineering at Sungkyunkwan University, Suwon, Korea. His research interests include power management ICs, charger designs and high-voltage gate drivers.

Jaejin Kim received his B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, Korea, in 2021 and 2023, respectively. He is currently an IC Design Engineer with Wavepia Inc., Hwaseong, Korea. His research interests include power management ICs and PLLs for memory systems.

Gunmo Koo received his B.S. and M.S. degree in electronics engineering from Kyungpook National University, Daegu, Korea, in 2022 and 2024, respectively. He is currently an IC Design Engineer with Samsung Electronics, Hwaseong, Korea. His research interests include power management ICs and PLLs for memory systems.

Kunhee Cho received the B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2007 and 2009, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Texas at Austin, Austin, TX, USA, in 2016. From 2009 to 2012, he was with the Fairchild Semiconductor, Bucheon, South Korea, where he designed power management integrated circuits (ICs). In 2015 and 2016, he was a Graduate Research Intern with the Texas Instruments Incorporated, Dallas, TX, USA, in the low-power RF team. From 2017 to 2020, he was with Qualcomm Technologies Incorporated, Santa Clara, CA, USA, where he designed power management ICs for battery charger systems. From 2020 to 2025, he was an Associate Professor with Kyungpook National University, Daegu, South Korea. In 2025, he joined Sungkyunkwan University, Suwon, South Korea. His research interests include power management ICs, high-voltage gate drivers, class-D amplifiers, and RF power amplifiers. Dr. Cho was a recipient of the Texas Instruments Outstanding Student Design Award in 2013.