

Gate Edge Sidewall Integration for Breakdown Voltage Enhancement in GaN HEMTs

Sang Woo Park, Jongmin Lee*, and Jang Hyun Kim*

Abstract: This study proposes a silicon nitride (Si_3N_4) sidewall structure for Gallium Nitride (GaN) high electron mobility transistors (HEMTs). The proposed structure effectively mitigates electric field (e-field) crowding at the gate-to-drain edge, a critical issue that leads to increased gate leakage and limited breakdown voltage (BV). Conventional GaN HEMTs suffer from severe e-field concentration, which requires effective mitigation strategies beyond conventional field plate (FP) that introduce undesirable parasitic capacitances. Our proposed sidewall structure effectively reshapes the gate edge profile, leading to a distribution of the e-field and improved device performance without requiring additional FP. The sidewall structure demonstrated a 34.76% reduction in peak e-field (from 20.13 MV/cm to 13.13 MV/cm) at the gate-drain edge compared to the conventional structure through TCAD simulations. This effective field mitigation resulted in a notable 8.8% enhancement in BV, increasing from 373 V to 406 V, and effectively suppressed gate leakage current near the BV. These results demonstrate that gate-edge sidewall engineering effectively alleviates e-field crowding, leading to improved breakdown performance and enhanced reliability in GaN HEMTs.

Index terms: GaN HEMT, sidewall, breakdown voltage, reliability, TCAD simulation

I. INTRODUCTION

Gallium nitride (GaN) high electron mobility transistors (HEMTs) have been widely investigated for power electronics and RF applications due to their wide bandgap (3.4 eV), high electron mobility, and high breakdown voltage (BV) [1-8]. Such material properties allow GaN HEMTs to achieve higher power density, faster switching, and greater efficiency than conventional silicon-based devices [9-13]. These advantages make Metal-Insulator-Semiconductor (MIS) GaN HEMTs attractive for high-voltage and high-efficiency power applications. However, MIS-GaN HEMTs still suffer from strong electric field (e-field) crowding at the gate-to-drain edge under high drain bias conditions as shown in Fig. 1(a) [14-18]. This

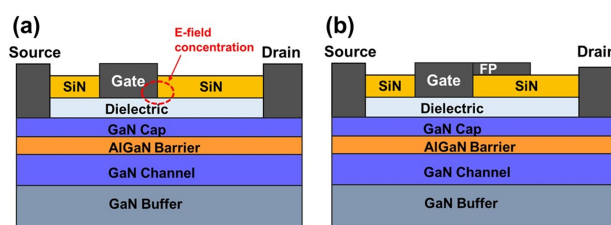


Fig. 1. Cross-sectional views of GaN HEMT structures. (a) Conventional MIS-GaN HEMT with electric field concentration near the gate edge. (b) Field plate (FP)-integrated structure for electric field distribution improvement.

phenomenon is caused by the sharp curvature at the gate edge, which induces a non-uniform potential distribution and leads to e-field crowding in the gate-to-drain region [19]. This highly localized e-field results in excessive gate leakage current and restricts the use of GaN HEMTs in high voltage applications. To mitigate this problem, field-plate (FP) structures shown in Fig. 1(b) have been widely adopted to distribute the e-field and suppress gate leakage [20-24]. However, FP integration inevitably increases parasitic capacitance due to the extended gate-to-drain overlap [25-29]. This parasitic capacitance leads to increased

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Department of Intelligence Semiconductor Engineering, Ajou University Suwon, Korea

E-mails : janghyun@ajou.ac.kr, jongmin@ajou.ac.kr

(*Corresponding author: Jang Hyun Kim, Jongmin Lee)

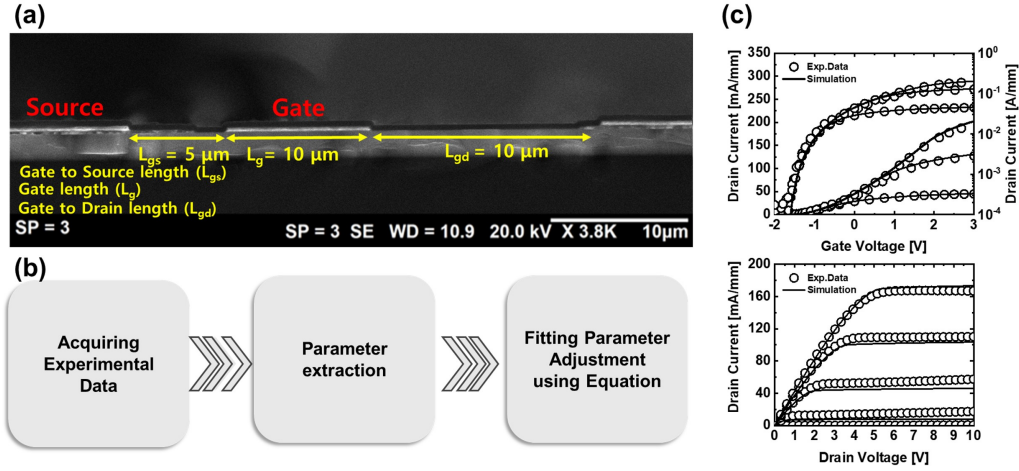


Fig. 2. (a) Structural dimensions of the fabricated reference MIS-GaN HEMT without sidewall spacer. (b) Measurement-based parameter extraction from CV and TLM (c) Calibration results of transfer and output curves comparing experiment and simulation.

switching losses and complicates device optimization for power applications [30–34]. In contrast, sidewall spacers formed at the gate edge provide an effective means to reshape the gate profile and mitigate e-field crowding near the gate-to-drain edge, without the need for additional FP. In this work, we propose and investigate a silicon nitride (Si_3N_4) sidewall structure integrated at the gate edge of MIS-GaN HEMTs. The effectiveness of the proposed structure is evaluated through TCAD simulation using parameters extracted from capacitance-voltage (C-V) and transmission line method (TLM) measurements of fabricated MIS-GaN HEMTs, and the transfer and output characteristics were calibrated to the measured devices, as shown in Fig. 2. The proposed structure is to employ a sidewall spacer that reshapes the gate edge profile and alleviates the sharp curvature. By modifying the gate geometry, the sidewall distributes the e-field in the gate-to-drain region and thereby reduces e-field crowding. This approach is intended to achieve these benefits without compromising the intrinsic device characteristics. These findings confirm that gate edge sidewall engineering can effectively suppress e-field crowding and leakage current, thereby offering a promising design strategy for achieving high breakdown capability and improved reliability in GaN HEMTs.

II. SIMULATION SETUP

The TCAD simulations were calibrated to match the measured characteristics of the fabricated MIS-GaN HEMTs. Surface donor-like interface traps were ex-

tracted from AC C-V measurements using the frequency-dependent conductance method [35]. In this approach, the onset voltage of the second rising slope in the AC-CV curves was tracked as a function of measurement frequency, and the resulting frequency-dependent shift was analyzed to obtain the corresponding trap energy range and interface-trap density. Through this procedure, a donor-like trap density of $2.56 \times 10^{13} \text{ cm}^{-2}$ located at 0.39 eV below the conduction band edge was determined. The source/drain contact resistance was obtained from TLM structures as $121.1 \text{ m}\Omega\text{-cm}^2$, and these experimentally extracted values were used to fine-tune the TCAD parameters so that the simulated current characteristics match the measurements. The calibrated parameters and physical models are summarized in Tables 1 and 2.

III. DEVICE STRUCTURE & PROCESS FLOW

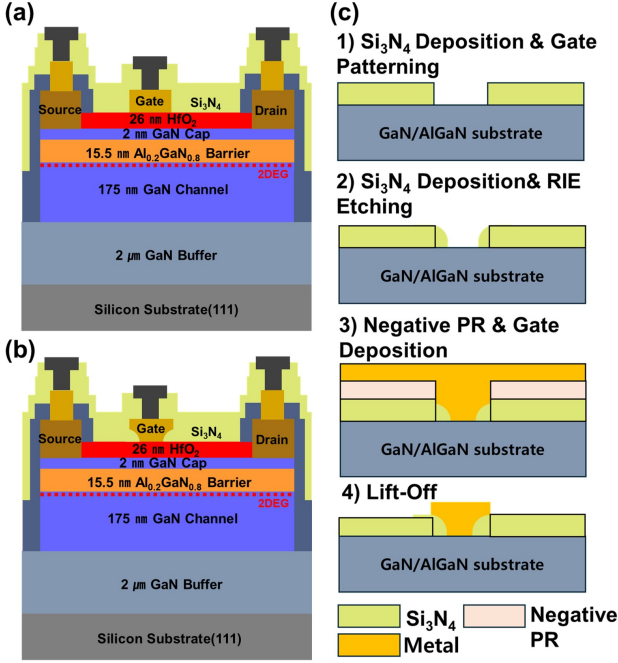
Fig. 3(a) illustrates a cross-sectional schematic of the conventional MIS-GaN HEMT, showing the fabricated device with a GaN/AlGaIn channel grown on a silicon substrate. The device is designed with a gate length (L_g) of $10 \mu\text{m}$ a source-gate spacing (L_{gs}) of $5 \mu\text{m}$, a gate-drain

Table 1. Simulation parameters.

Parameter	Value	Description
D_{it}	$2.56 \times 10^{13} \text{ cm}^{-2}$	Surface donor-like trap density
μ_n	$1900 \text{ cm}^2/\text{V}\cdot\text{s}$	Electron mobility in GaN
R_c	$121.1 \text{ m}\Omega\text{-cm}^2$	Contact resistance
V_{sat}	$1.8 \times 10^7 \text{ cm/s}$	GaN saturation velocity

Table 2. Physical model used in simulation.

Category	Model	Description
Mobility	High-field saturation mobility model	Accounts for velocity saturation
Recombination	Shockley-read-hall (SRH)	Models deep-level traps
Polarization	Spontaneous, piezoelectric polarization	Determines 2DEG formation
Impact Ionization	van Overstraeten-de Man	Breakdown voltage modeling

**Fig. 3.** (a) Cross-sectional schematic view of conventional MIS GaN HEMT, (b) and Side-Wall HEMT. (c) Process flow illustrating the formation of sidewall spacers.

spacing (L_{gd}) of 15 μm , and a gate width (W_g) of 200 μm .

The epitaxial stack consisted of a 2 μm GaN buffer, a 175 nm GaN channel, and a 15.5 nm AlGaIn barrier layer, a 2 nm undoped GaN cap layer. After RCA cleaning, the active area was patterned and etched by inductively coupled plasma - reactive ion etching (ICP-RIE) using a Cl_2/BCl_3 gas mixture for 40 seconds to form device isolation. The source/drain contacts were formed with Ti/Al/Ni/Au (20/120/55/45 nm) deposited by electron beam (e-beam) evaporation, followed by annealing at 860°C for 90 seconds. A 26-nm thick HfO_2 gate dielectric was deposited on the device by atomic layer deposition (ALD), and the HfO_2 above the source and drain region was then selectively removed by ICP-RIE. Gate and pad electrodes were formed by depositing Ni/Au (320

nm). A Si_3N_4 passivation layer thickness of 350 nm was then deposited by plasma-enhanced chemical vapor deposition (PECVD) and etched by coupled reactive ion etching (CCP-RIE) with CF_4/O_2 gas mixture 90 seconds. Finally, Al/Au (370 nm) was deposited by e-beam evaporation to complete the device fabrication. As shown in Fig. 3(b), the sidewall HEMT follows the same process flow as the MIS-HEMT, with the sidewall formation step additionally included. The sidewall spacer formation process is illustrated in Fig. 3(c). A Si_3N_4 layer was deposited and patterned to define the gate, followed by an additional Si_3N_4 deposition and etching to form the sidewall. The gate metal was deposited, and the structure was completed by lift-off process.

IV. RESULTS AND DISCUSSION

In conventional MIS-GaN HEMTs, the gate-to-drain edge is known to be the most critical region for e-field crowding. At this region, the high curvature of the gate corner leads to a strong localization of the e-field under high drain bias. The proposed sidewall HEMT structure modifies the gate-edge e-field distribution, thereby suppressing crowding at the gate-to-drain region. In this structure, the Si_3N_4 sidewall spacer has a lateral extension and vertical height of 0.1 μm each, and its outer corner is rounded with a radius of 0.3 μm . Fig. 4(a) shows the lateral e-field profile gate-to-drain edge at gate voltage (V_{gs}) = -2 V and drain voltage (V_{ds}) = 355 V. The conventional device exhibits a sharp peak of 20.13 MV/cm due to e-field crowding, whereas the sidewall-integrated device reduces the peak to 13.13 MV/cm, corresponding to a 34.8% reduction in e-field intensity. This result confirms that the proposed sidewall structure effectively relaxes the gate-to-drain edge e-field enhancement under BV conditions. Fig. 4(b) shows the impact-ionization rate along the 2DEG channel. In the sidewall device, the impact-ionization rate at the gate-to-drain edge is reduced compared with the conventional structure, consistent with the e-field mitigation in Fig. 4(a). The mitigation of the gate-to-drain edge field crowding makes the lateral electric field in the drift region slightly more uniform, which causes the channel region around $x = 20\text{-}30 \mu\text{m}$ to exhibit a slightly higher impact-ionization rate than in the conventional device. However, this value remains much lower than the peak at the gate-to-drain edge and does not change the breakdown location or the breakdown voltage. These trends are further illustrated in the two-dimensional electric-field dis-

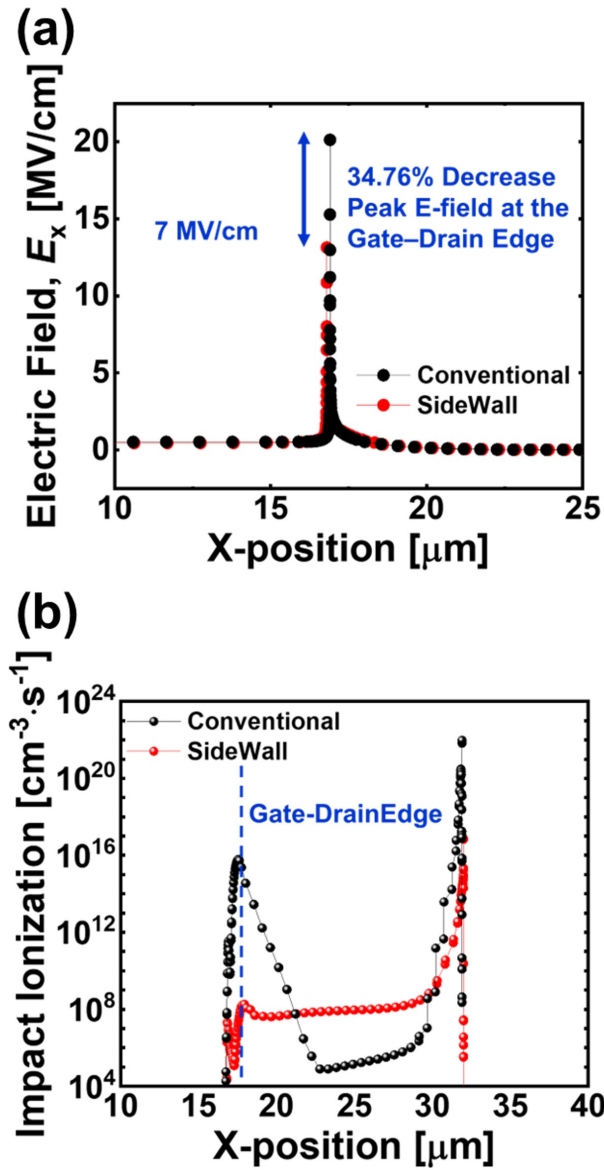


Fig. 4. (a) Lateral electric field along the gate-drain edge at $V_{gs} = -2$ V and $V_{ds} = 355$ V, showing 34.76% peak electric field reduction from 20.13 to 13.13 MV/cm. (b) Impact ionization profiles for conventional and sidewall structures under same bias.

tributions shown in Fig. 5. In the conventional device, the peak e-field is highly concentrated at the gate corner, which critically affects the breakdown characteristics. In contrast the sidewall-integrated structure distributes the e-field toward the spacer region, resulting in a more uniform profile near the gate-to-drain edge. The output and transfer characteristics are investigated to confirm the intrinsic device behavior. Figs. 6(a) and 6(c) present output characteristics with V_{ds} swept up to 10 V and V_{gs} varied from -2 V to 2 V in 1 V steps for the conventional and sidewall de-

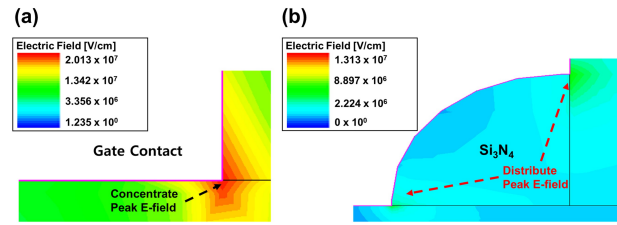


Fig. 5. Electric field distribution near the gate-drain edge for (a) the conventional structure and (b) the sidewall structure.

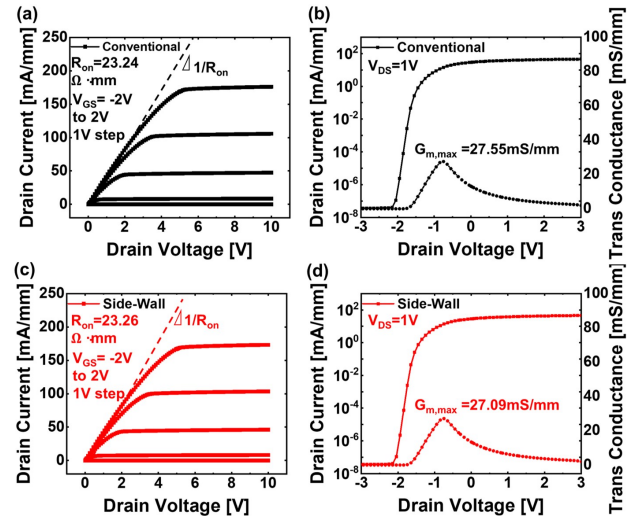
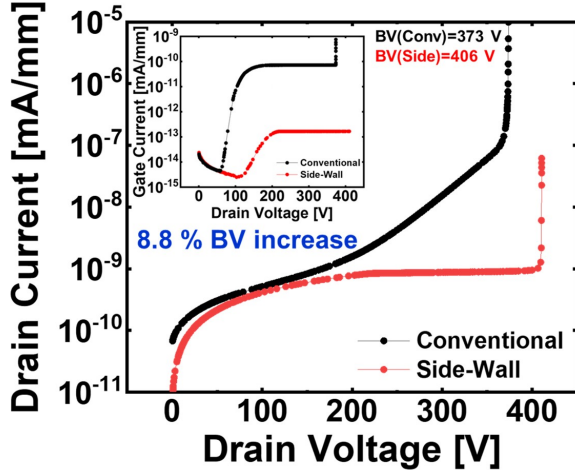


Fig. 6. Conventional structure (a) output curve and (b) transfer curve. Sidewall structure (c) output curve and (d) transfer curve.

vices, respectively. Both devices exhibit comparable output characteristics, with extracted R_{on} (on-resistance) of 23.24 $\Omega \cdot \text{mm}$ and 23.26 $\Omega \cdot \text{mm}$. Figs. 6(b) and 6(d) show the transfer characteristics of the conventional and sidewall structures at $V_{ds} = 1$ V. The conventional structure exhibits a maximum transconductance ($G_{m,max}$) of 27.55 mS/mm, while the sidewall-integrated structure demonstrates a comparable value of 27.09 mS/mm. These similar intrinsic electrical characteristics are consistent with the fact that the sidewall extends by about 0.1 μm on each side of the 10- μm gate, corresponding to about a 2% change in gate length. As a result, the 2DEG sheet density and mobility under the gate remain very similar in the two devices, and the sidewall mainly distributes the off-state electric field at the gate-to-drain edge region. Consequently, the proposed sidewall structure improves the breakdown voltage while maintaining nearly identical intrinsic electrical characteristics, with only a slight reduction compared to the conventional device. The BV characteristics of conventional and sidewall-integrated de-

Table 3. Breakdown voltage and DC characteristics as a function of sidewall dimensions.

Structure	Lateral extension (μm)	Height (μm)	BV [V]	R_{on} [$\Omega\text{-mm}$]	V_{th} [V]	$G_{\text{m,max}}$ [mS/mm]
Sidewall (0.1 μm / 0.1 μm)	0.1	0.1	406	23.26	-1.42	27.09
Sidewall (0.2 μm / 0.2 μm)	0.2	0.2	406	23.24	-1.42	27.16
Sidewall (0.3 μm / 0.3 μm)	0.3	0.2	406	23.21	-1.42	27.24

**Fig. 7.** BV characteristics with 8.8% improvement by sidewall. Inset: Gate leakage rise near BV in conventional structure.

vices are compared in Fig. 7. The conventional MIS-GaN HEMT exhibits a BV of 373 V, while the sidewall device achieves 406 V, corresponding to an 8.8% improvement. This enhancement is attributed to the distribution of the e-field away from the gate corner, as demonstrated in Figs. 4 and 5, which reduces the peak e-field intensity at the gate-to-drain edge. As a result, the impact ionization is delayed, and the device sustains a higher drain bias before reaching breakdown. In addition to the improvement in BV, the gate leakage behavior near BV also shows a distinction between the two structures. As shown in the inset of Fig. 7, the conventional device exhibits a steep rise in gate leakage current as the BV point is approached, which is consistent with the strong e-field crowding at the gate-to-drain edge. In contrast, the sidewall-integrated structure significantly suppresses this leakage increase, indicating that the distributed e-field not only enhances the breakdown strength but also improves gate reliability under high voltage conditions. Table 3 summarizes the dependence of the breakdown and intrinsic electrical characteristics on the sidewall dimensions. When the lateral

extension and height of the sidewall are increased from 0.1 μm to 0.3 μm , the BV remains at 406 V, while R_{on} changes only slightly from 23.26 $\Omega\text{-mm}$ to 23.21 $\Omega\text{-mm}$ and $G_{\text{m,max}}$ from 27.09 mS/mm to 27.24 mS/mm, with V_{th} fixed at -1.42 V. These results indicate that 0.1 μm sidewall is already sufficient to modulate the e-field at the gate-to-drain edge. Increase the sidewall thickness to induce no further change in the e-field peak at the gate-to-drain edge, and the channel potential profile does not change. These results demonstrate that the proposed sidewall approach provides an effective means of improving device reliability, while causing only a slight degradation in the intrinsic electrical characteristics.

V. CONCLUSIONS

In this work, a sidewall structure was proposed and investigated to suppress e-field crowding in MIS-GaN HEMTs. The sidewall integration effectively reduced the peak e-field at the gate-drain edge by 34.8%, thereby alleviating impact ionization and mitigating gate leakage near breakdown. As a result, the BV was improved from 373 V to 406 V, corresponding to an 8.8% enhancement, while the output and transfer characteristics remained nearly identical to those of the conventional device. These findings confirm that sidewall engineering provides a practical design strategy to enhance breakdown performance and device reliability, with only a slight degradation in the intrinsic electrical characteristics.

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Sang Woo Park received the B.S. degree in the Department of Electrical Engineering from Ajou University, Suwon, Korea, in 2024. He is currently pursuing an M.S degree in the Department of Intelligence Semiconductor Engineering, Ajou University, Suwon, Korea. His research interests include GaN-based power devices, device reliability, and E-mode GaN HEMTs.



Jongmin Lee (Member, IEEE) received the B.S. degree in semiconductor systems engineering and the Ph.D. degree in electrical and computer engineering from Sungkyunkwan University, Suwon, Korea, in 2017 and 2022, respectively. From 2022 to 2023, Dr. Lee was affiliated with Samsung Electronics as an Engineer. In 2023, he joined Ajou University, Suwon, Korea, as an Assistant Professor for the Department of Intelligent Semiconductor Engineering. His research interests include hardware security, post-quantum cryptography accelerators, and low power digital circuits and systems.



Jang Hyun Kim (Member, IEEE) received the B. S. degree in electrical and electronic engineering at Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2009. He received his M.S. and Ph.D. degrees in electrical engineering from Department of Electrical and Computer Engineering at

Seoul National University, in 2011 and 2016, respectively. After acquiring his Ph.D. degree, he worked as a Development Researcher for DRAM at SK hynix from September 2016 to February 2020. He served as an Assistant Professor in the Department of Electrical Engineering at Pukyong National University from March 2020 to February 2023. He has been working as an Assistant Professor in the Department of Electrical and Computer Engineering at Ajou University since March 2023. His current research interests include advanced logic semiconductor devices and power semiconductor devices.